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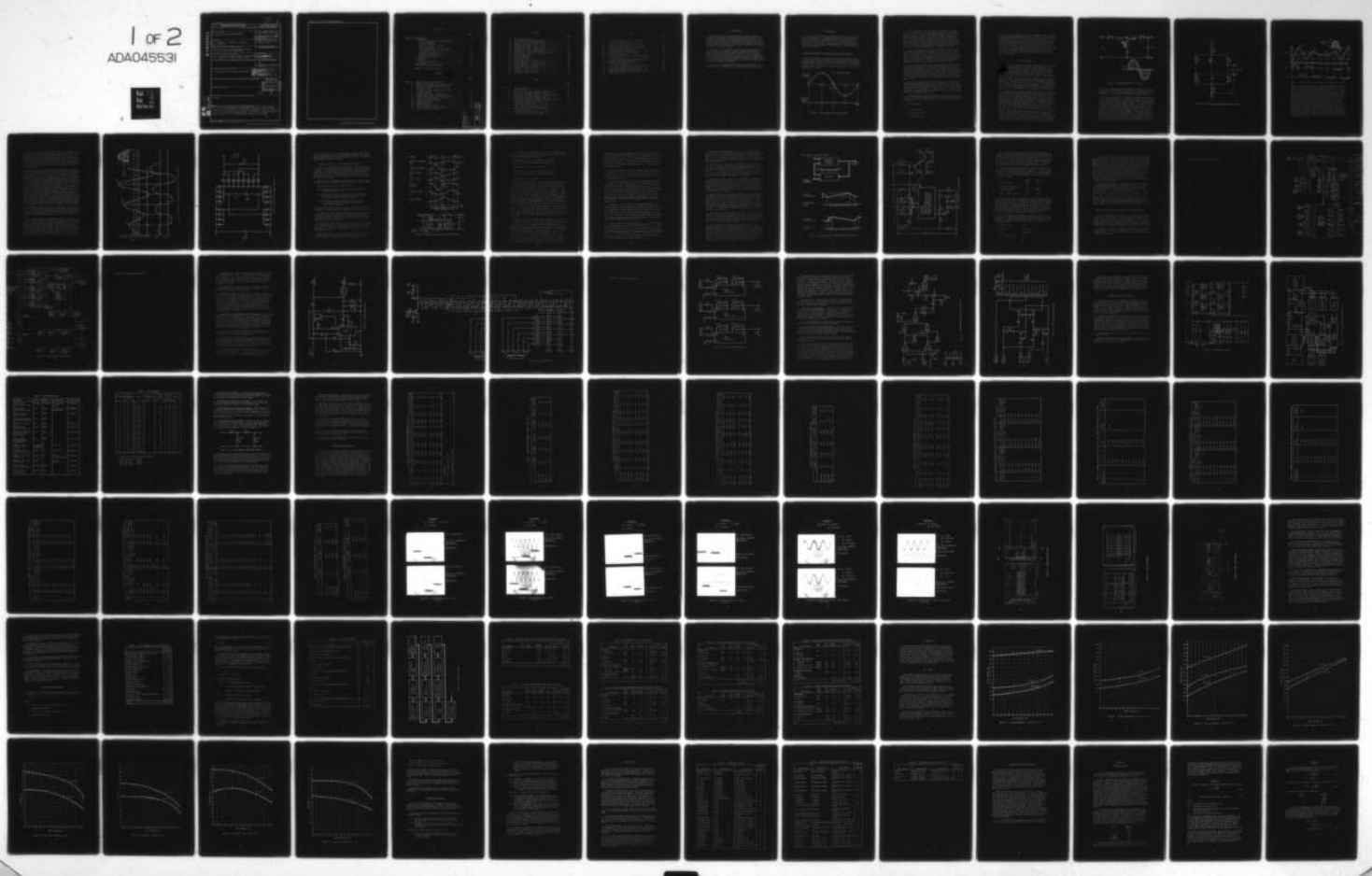

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The results of investigations on inverter designs based on high frequency waveform synthesis techniques are described. Two specific circuits based on the use of resonant circuits are discussed in detail. Test data on a small scale prototype breadboard is presented. A full scale 3.0 kilowatt three phase design based on the breadboard configuration is described.

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1. INTRODUCTION

This report describes inverter design techniques pertaining to 60 and 400 Hz sinewave power generation by means of high frequency synthesis. The inverter configurations described achieve the desired waveform synthesis in a single power processing stage. Regulation to remove the effects of load and input voltage variations is accomplished by controlling the quantity of controlled energy pulses delivered to the output circuit.

The design of a 3.0 kilowatt, three phase inverter based on the most promising high frequency synthesis technique is described. This design uses five 300-W modules per phase to provide the required 1.0 kilowatt output power per phase. It also provides the increased capability necessary to support additional VA requirements at 0.8 power factor and 120% overload. A conceptual design of the 3.0 kilowatt inverter is discussed and the results of packaging and reliability analyses are presented.

Test data on a 100-W breadboard unit are also presented. The breadboard unit was subjected to a detailed performance evaluation.

2. INVESTIGATION

The technique of high frequency waveform synthesis as applied to inverter design refers to sinusoidal waveform construction by the controlled transfer of energy-limited pulses to an output capacitive storage element. The inverter load is connnected across the capacitive storage element. The energy pulses are delivered to the capacitor and load combination at high frequency to limit ripple to an acceptable level.

General Considerations of High Frequency Waveform Synthesis

Figure 1 illustrates a sinewave voltage synthesized by trains of constant energy pulses occurring with a sinusoidal time distribution. A smooth voltage waveform is obtained by using a filter. The product of maximum pulse repetition rate, f_r, and pulse energy, E, determines the maximum power available at the peak of the output voltage waveform according to $P_m = f_r E$.

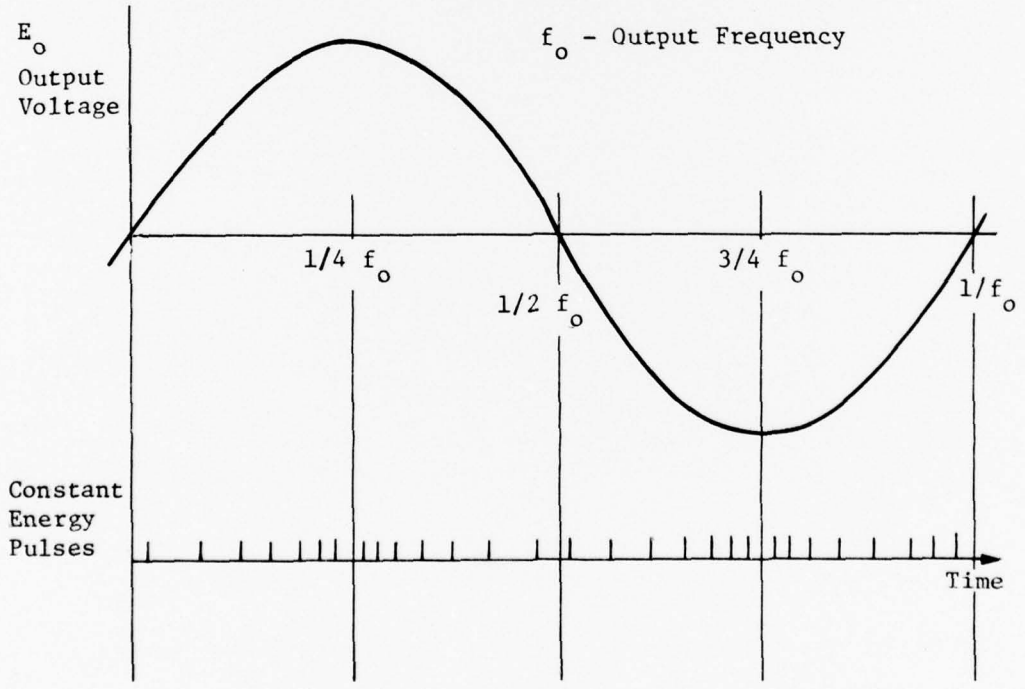

Figure 1. High frequency waveform synthesis.

Voltage regulation is obtained by gating the constant energy pulses as a function of the error between the output voltage and a reference sinewave voltage. Regulating capability depends on the number of pulses per cycle of the output voltage. For example, fewer than 100 pulses per half-cycle can be expected to give worse than ±1% voltage regulation, because each pulse is capable of delivering 1% of the energy required per pulse period at the peak of the output voltage. Because high frequency, low energy pulses provide fine voltage resolution, high pulse repetition frequency also eases the filtering requirement for low distortion waveform.

A practical limitation on repetition frequency is set by the switching characteristics of the physical circuit elements. Power losses in switching diodes, SCRs and transistors increase with operating frequency. Although the reactive components in filters decrease electrically and in physical size with frequency, the power loss in these components, particularly inductors and transformers, increases with frequency. Therefore, high operating frequency is, in general, obtained at the expense of inverter efficiency.

For an inverter employing high frequency synthesizing techniques, the design of the output filter is determined largely by the requirements for waveform at light loads. As output power reduces to zero, fewer pulses are required until, at zero load, the regulator allows only enough pulses to pass to supply losses in the inverter. For this reason, the filter consists of a capacitor in parallel with an inductor. This combination is resonant at the output frequency of the inverter. This type of filter provides good waveform regardless of load.

Immunity to changes of the load power factor is provided by the parallel resonant output filter. For a lagging power factor, this is done by making the filter inductance small compared to the equivalent parallel load inductance by a factor of 2 or 3. This also ensures that the filter capacitor is small compared to the equivalent parallel load capacitance for a leading power factor of the same magnitude as the lagging power factor.

A disadvantage of the parallel resonant filter is its physical size for low inverter output frequencies. Waveform at all loads and immunity to power factor improve with reduced damping where damping is defined as

$$D = (1/2R)(L/C)^{\frac{1}{2}}$$

and

R = load resistance

L = filter inductance

C = filter capacitance

Hence, for low damping, the reactive components have to be electrically and physically large relative to the load. The circulating current between reactive elements in the filter increases with reduced damping. This also leads to increased physical size. This problem is somewhat relieved because, for a given pulse repetition frequency, the damping at low inverter frequency does not need to be as low as necessary at high inverter frequency. For example, at 400 Hz, D = 0.2 is suitable provided the power factor is no lower than about 0.8; however, higher damping such as D = .6 can be used at 60 Hz. The increased damping at 60 Hz is permissible because more pulses are available per output waveform period to fine tune the waveform shape.

Inverter Concept I

Figure 2 shows a method of achieving high frequency waveform synthesis by using a resonant power stage. The operation of the circuit can be illustrated by considering a single energy transfer cycle. Assume the initial voltages on the capacitors and the initial current in the inductor are zero. When switch S1 is closed, current i_1 will flow into the resonant L1-C1 network and capacitor C1 will be brought to a peak voltage equal to $2\ E_{in}$. At the same time, the current i_1 will fall to zero. At this time S1 is opened and S2 is closed. Energy stored on C1 is then delivered to C2 by current i_2. The current i_2 will increase in sinusoidal fashion and then decrease to zero. When i_2 falls to zero, S2 is opened and the cycle is complete. Energy has been transferred to the output capacitor C2 by a two stage process: (1) energy from the source was delivered to C1, (2) the energy on C1 was transferred to the output.

An extension of the elemental power stage (Figure 2) to a power stage providing both positive and negative voltage for the alternating polarity of the output waveform is shown in Figure 3. The switches in Figure 3 are represented by silicon-controlled rectiviers (SCRs). A single cycle of operation of the circuit shown in Figure 3 begins, as for the previous case, by transferring energy from the source to the resonant network L1-C1. Assume the initial conditions on the reactive components are zero. The resonant network L1-C1 is connected to the source by turning on Q1 and Q6. If the voltage drop in Q1 and Q6 is negligible, capacitor C1 will charge to $2E_{in}$. At the time the C1 voltage peaks, the current drawn from the source will attempt to reverse. However, it will be prevented from reversing because the SCR switches, Q1 and Q6, will automatically turn off. The energy stored on C1 can now be delivered to the output capacitor C2 through two alternative paths depending on the output polarity desired. One path is obtained by simultaneously closing Q3 and Q4. A closed loop is then formed with L1,

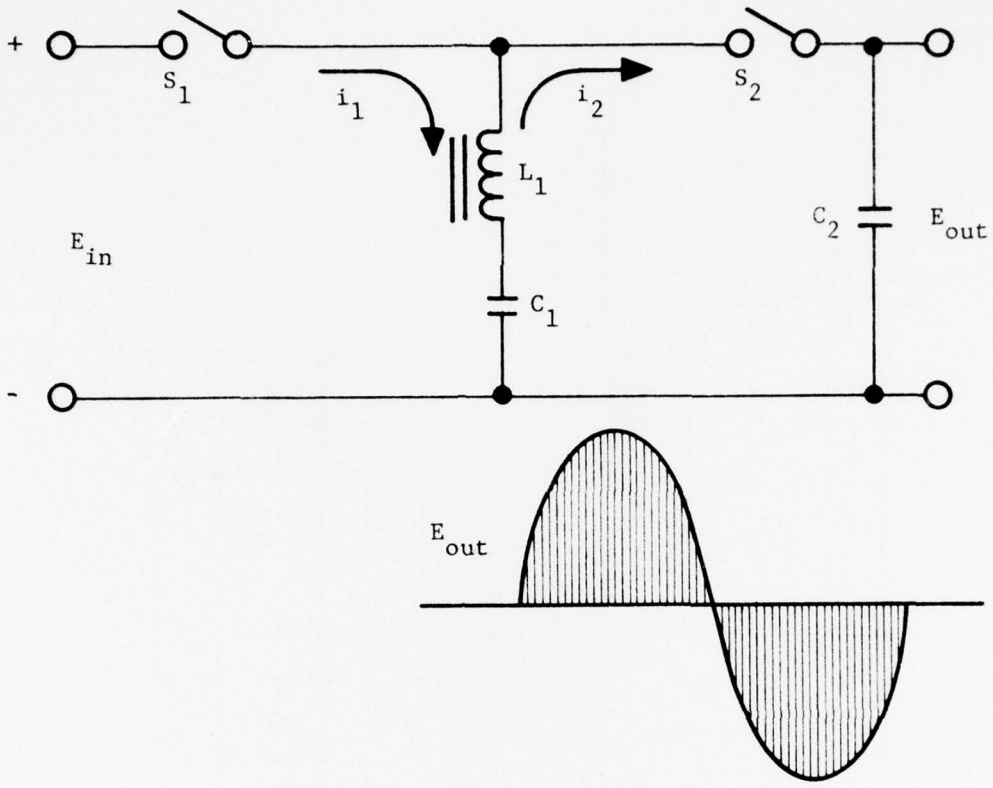

Figure 2. Resonant power stage - Concept I.

C1, and C2 in series and current will flow to charge C2. If Q2 and Q5 were closed instead of Q3 and Q4, then a similar closed loop containing L1, C1, and C2 in series would be established but with C2 reversed. C2 would then be charged with opposite polarity.

The circuit in Figure 3 is capable of delivering energy to the load for both polarities of the output waveform. It is an impractical configuration, however, since it can be shown to be uncontrollable for repetitive energy transfer cycles. For operation through a single half cycle of the output waveform, the circuit of Figure 3 can be represented by the elemental circuit of Figure 2 with switches Q1 and Q6 represented by S1 and switches Q3 and Q4 (or Q2 and Q5 as the case may be) represented by S2. The initial conditions on the reactive circuit elements L1, C1, and C2 will not, in general, be zero. A representative case is shown in Figure 4 where the input voltage is initially 40V, the output voltage is 60V, and capacitor C1 voltage is -40V. When switch S1 is closed, C1 will charge to 120V, at which time S1 opens and S2 closes. Energy is then delivered to C2, and C1 discharges to zero. At this

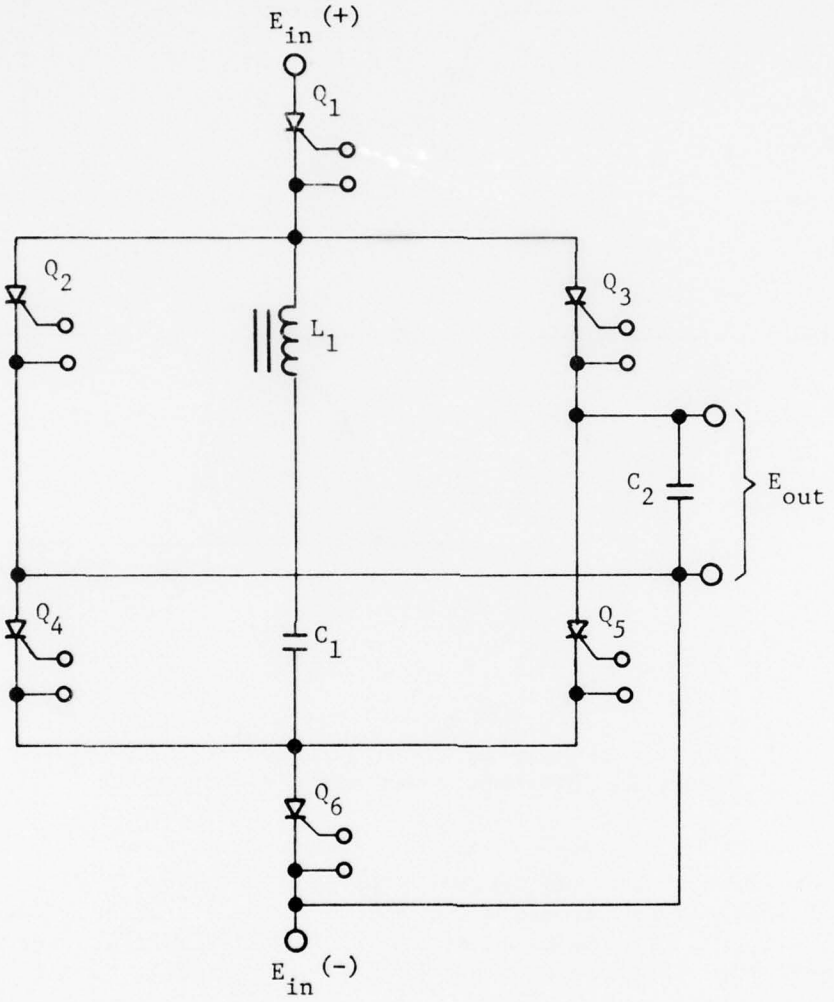

Figure 3. Power stage providing dual polarity output.

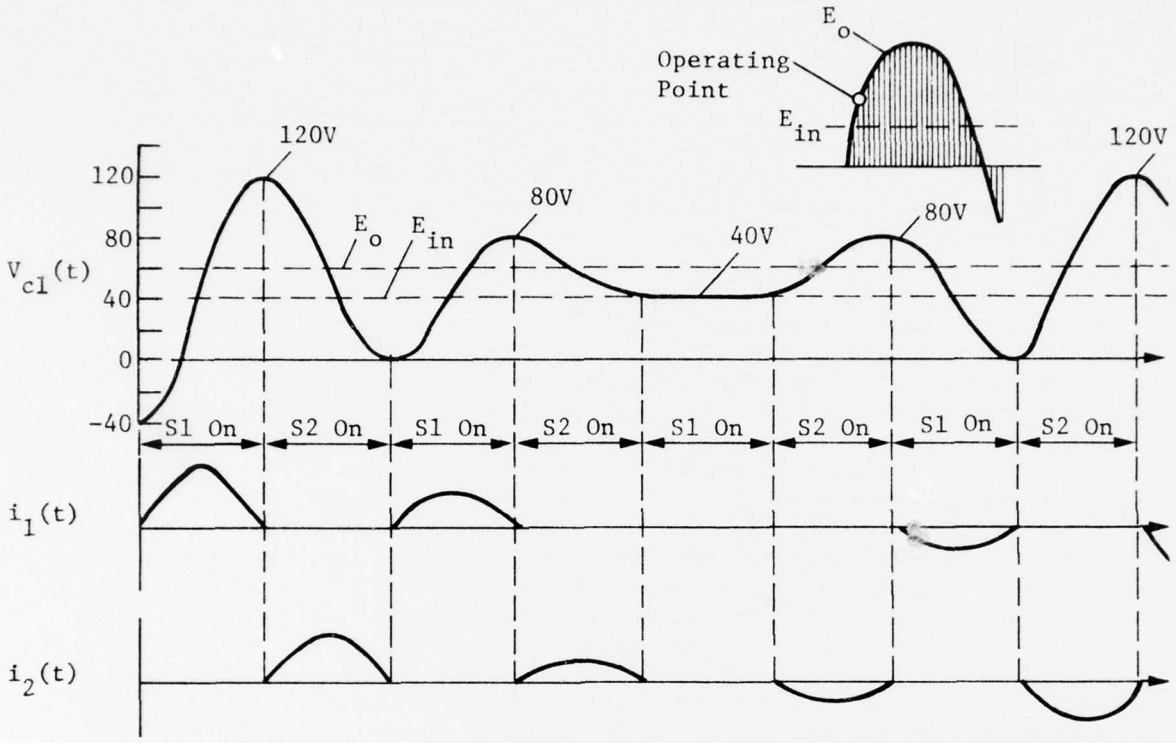

Figure 4. Operation for input voltage less than output voltage.

time S2 opens and S1 closes. C1 is again charged from the source but only to 80V, substantially less than on the first cycle. When S2 is next closed, energy is again delivered to C2, but less than for the previous cycle, and C1 is only discharged to 40V. When S1 next closes, no energy is transferred to C1 from the source since they are both at 40V and no driving voltage is established across inductor L1. When S2 then closes, the output voltage across C2 is greater than the voltage on C1 and energy is removed from the load and transferred to C1 which charges to 80V. In the next closure of S1, energy is being transferred from C1 back to the source; thus energy flow has reversed. Energy is being removed from the load and transferred to the source rather than vice versa as required. In general, whenever the output voltage is greater than the input voltage, this condition will occur. Hence, to maintain energy flow from source to load, the input voltage must be greater than the output voltage. If the available source voltage is less than the desired output voltage, then a boost preregulator is required ahead of the inverter stage to assure proper energy flow from source to load.

While a preregulator could be added ahead of the inverter stage to assure proper energy flow, the inverter circuit of Figure 2 will still be impractical because the energy transfer per pulse is uncontrollable. Figure 5 illustrates this situation by showing an operating point with the output voltage less than the input voltage. Rather than the circuit voltages and currents decreasing and reversing phase as for the previous case, they now increase uncontrollably on successive cycles. In a practical inverter, this uncontrollable growth tendency would lead to overstress and destruction of the circuit elements.

To resolve the operational problems discussed above and recover control of the inverter power stage, it is necessary to add additional switch elements to the circuit. The required modifications are shown in Figure 6. The circuit shown can be designed to deliver controlled energy pulses to the output even for source voltages less than the output voltage, thus eliminating the need for a preregulator. This capability is achieved by adding switching elements that allow the resonant circuit L1-C1 to be charged in steps. For example, closing Q5, Q6, Q13, and Q14 will charge C1 to a certain voltage. If this voltage is less than the output voltage, energy cannot be delivered and C1 must be charged further. This is accomplished by closing Q1, Q2, Q9, and Q10 and reconnecting the resonant circuit L1-C1 to the source but at opposite polarity. C1 will charge to a higher (but negative) voltage and acquire more energy. Next, Q5, Q6, Q13, and Q14 are closed and the resonant network is once more reversed and connected in a normal sense across the source. The capacitor acquires more energy and the voltage increases a third time. If the voltage on C1 is now higher than the output voltage, then energy can be transferred to the output by closing Q17 and Q23. If not, C1 can be pumped further until it attains a voltage greater than the output, at this time, the stored energy can be transferred.

The problem with circuit voltages and currents growing uncontrollably for source voltage greater than output voltage is similarly resolved. In this case, the resonant network L1-C1 is repetitively reversed and connected to the output circuit rather than to the source voltage as discussed above for source voltage less than output voltage.

While the inverter power stage shown in Figure 6 can, in principle, be made to work, it has serious drawbacks that limit its usefulness. The requirement for several reapplications of the resonant network to the source voltage before transferring energy to the load seriously limits the high frequencies necessary for quality waveform synthesis. Also, the circulating currents and voltages in the switches and resonant elements will, in general, be very much larger than those drawn by the output load. Hence, the circuit will have to process a large amount of reactive power relative to the real power it can deliver to a load. As a consequence, significant power

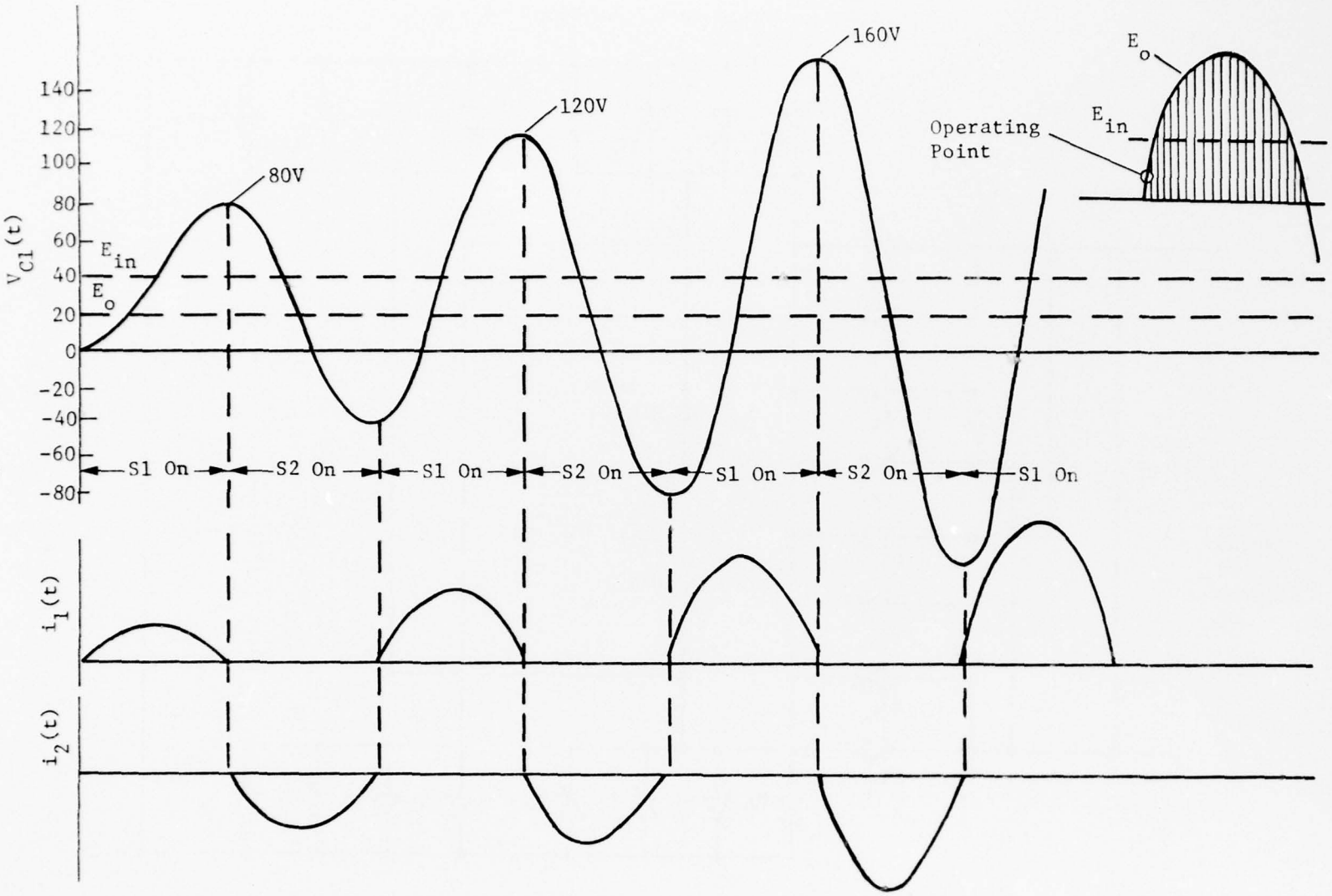

Figure 5. Operation for input voltage greater than output voltage.

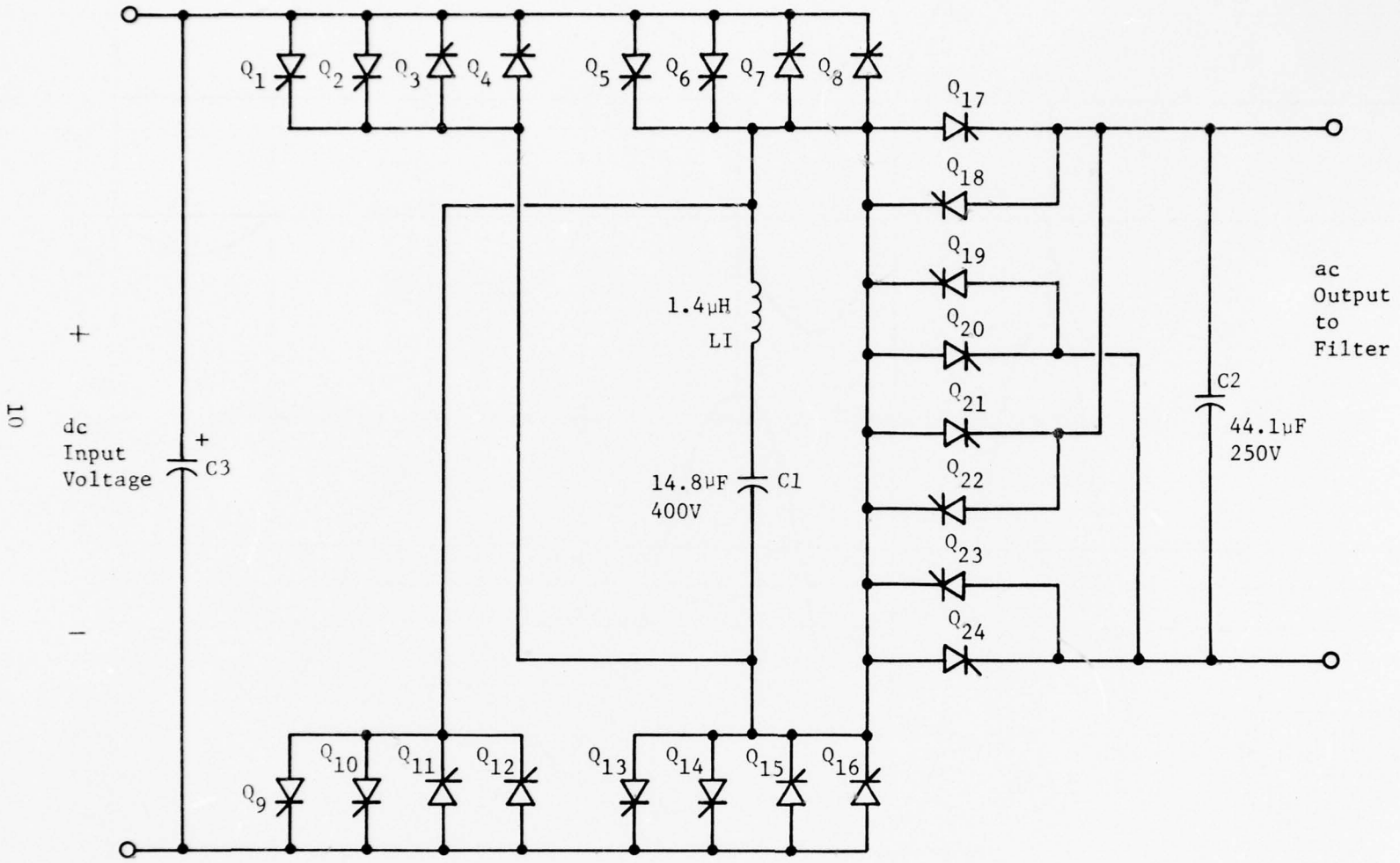

Figure 6. Complete power stage - Concept I.

loss will be realized in the circuit elements which degrade the inverter efficiency, and the circuit elements themselves will have to be oversized, relative to the output power obtained, to accommodate the high peak voltages and currents.

Inverter Concept II - Resonant Switching Inverter

An inverter power stage with better characteristics than those in Concept I was investigated. This inverter, a resonant switching inverter, is derived from a circuit technique developed and successfully applied for dc-dc power conversion. The operation of this power stage as a dc-dc converter will first be described and then followed by a discussion of the modifications required to adapt it for use as an inverter.

Figure 7 shows the schematic and waveforms of the power output stage of a resonant switching dc-dc converter with isolated output.

The essential features of the technique are:

(a) The collector current waveform of the power transistor resembles a half-sinusoid.

(b) The power transistor is turned on and saturated before the collector current begins to rise; it is turned off after the collector returns to zero.

(c) The collector current waveform and timing is due to two resonant circuits consisting of two inductors sharing the same capacitor.

The natural frquencies of the two resonant circuits, considered individually, are widely separated, usually by a factor of about four.

In addition to these essential features, the base drive current is obtained by positive feedback from a current transformer with its primary winding in the collector circuit. Thus the base current waveform is also a half-sinusoid coincident with and proportional to the collector current.

A description of a cycle of operation will illustrate the essential features and provide a background for understanding the advantages of the technique. The operating cycle falls naturally into three periods: (1) energizing period, (2) recovery period, (3) power output period.

The recovery period partially overlaps both the other two, and the power output period may extend into the energizing period. Figure 7 illustrates a converter running at full power.

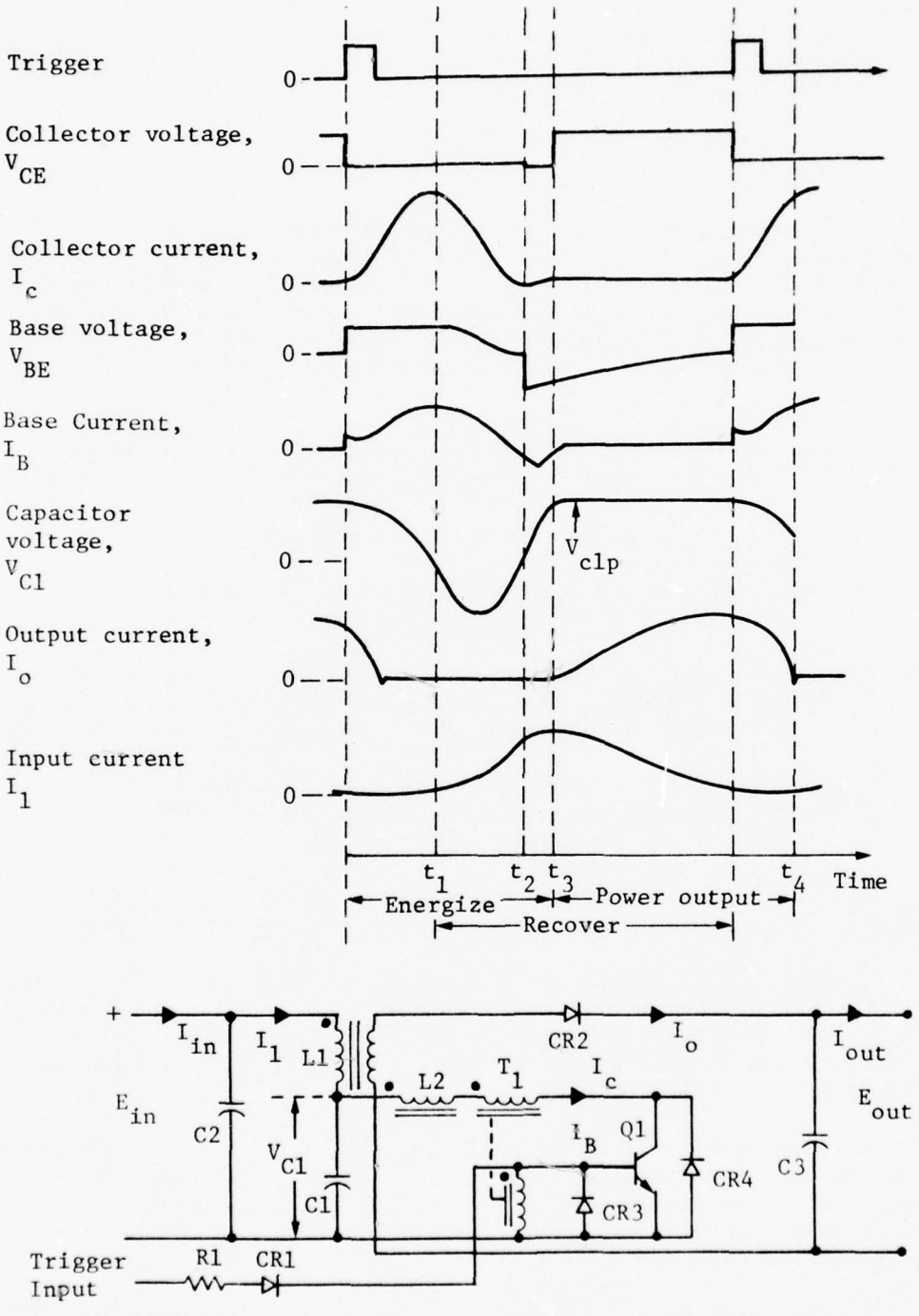

Figure 7. Resonant switch power stage and waveforms.

The energizing period covers the time, 0 to t_3, beginning with turn-on of the transistor by the leading edge of the trigger pulse. The conditions before zero time are:

Resonant capacitor, C_1 is charged to peak voltage, V_{C1P}, which is higher than the input voltage, E_i.

The inductor current, I_1, is at minimum.

Collector current, I_C, base current, I_B, and base voltage, V_{BE}, are all zero. L_2 has zero energy.

Output current, I_o, is flowing.

During this period inductor, L_1, is reenergized from the input filter, C_2, and from the source. This is done by an interchange of energy in the resonant circuit, L_2C_1. The action is as follows: at t_o the base-emitter voltage rises quickly to saturation. From t_o to t_2, I_c, under control by L_2C_1, rises sinusoidally to a peak and falls back to zero. By means of current transformer, T_1, the resonant circuit, L_2C_1, also controls base drive and the transistor is driven throughout this interval with a forced β of about 10. From t_0 to t_1, the resonant capacitor acts as a source and delivers all of its energy to establish I_c in L_2 and to drive the transistor. V_{C1} reaches zero and L_2 reaches peak energy at t_1. This increasing voltage is the potential that begins energizing L_1 and blocks the fast recovery rectivier, CR_2, so the output filter C_3, and the load have no effect on the circuit during the remainder of the energizing period.

During time t_0 to t_1, a slight rise in energy in L_1 is indicated by rising I_1 driven by $E_i - V_{C1}$. However, because of the phase of V_{C1} relative to I_C, I_1 is delayed about 90 degrees behind I_C. This completes the first part of the energizing period. In the second part of the energizing period, t_1 to t_2, there is a second change of energy in the high-frequency resonant circuit. As I_C falls toward zero, the energy in L_2 falls from its peak to zero. This energy charges C_1 in the reverse sense and drives the transistor. V_{C1} falls sinusoidally below zero. In this interval C_1 comes under a second influence current I_1 through L_1. This current is driven

by voltage $E_i - V_{C1}$, which increases as V_{C1} falls farther below zero. Meanwhile the first influence, I_C, is decreasing. About half way through the interval t_1 to t_2, the two influences cancel and V_{C1} reaches a minimum. Then the current, I_1, predominates over I_C and V_{C1} rises sinusoidally reaching zero at t_2. I_1 reaches a peak at approximately t_3.

In the interval t_2 to t_3, C_1 is energized, partly by the source and partly by L_1, from $V_{C1} = 0$ to V_{C1P}. This is the end of the energizing period. L_1 and C_1 are both at peak energy level ready to deliver output power.

The recovery period begins at t_1 in the energizing period and extends into the power output period. L_2 recovers during t_1 to t_2 by means of the reverse voltage excursion of V_{C1}. From t_2 to t_3, the current transformer, T_1, reacts from the drive that was applied by I_c and partially recovers the flux level it had before $t = 0$. In reacting it causes an undershoot in I_B and removes the stored charge from the base-emitter region. This completes recovery of the transistor. Recovery of T_1 is completed later in the power output period.

Also during t_2 to t_3 there may be a slight undershoot in I_C. This undershoot flows not through Q_1 but through the diode CR4. The combination of clamping by CR_4 and stored charge in the base-emitter prevents V_{CE} from rising, although V_{BE} is below zero and I_c is zero. At t_3, V_{CE} rises to V_{C1P} with practically no overshoot. Even with an overshoot there would be no switching dissipation in the collector circuit because I_C is zero.

L_1 must also recover from the voltage, $E_i - V_{C1}$, applied during approximately the latter two-thirds of the time, t_0 to t_3. This is done by the application of V_{C1P}, which is higher than E_i. V_{C1P} is usually high enough to allow the transistor to be run at about a 50% duty cycle. The maximum V_{C1P} is set by the rectifier, CR_2, clamping on E_{out} as I_o begins to flow. When running at full power, the recovery of L_1 occurs over the whole period t_3 to t_4.

During the power output period from t_3 to t_4, L_1 behaves as a reacting transformer delivering its energy to the output filter, C_3, and to the load. The falling energy level of L_1 is indicated by falling I_1. In cases where the load is light, I_0 is small and I_1 will cross zero and become negative. Negative I_1 indicates that the load is not accepting the energy and the energy is circulating back into the input filter C_2.

Figure 7 shows a case where the next trigger pulse occurs before L_1 has completely discharged its energy. Thus the power output interval overlaps into the following energizing period until V_{C1} falls sufficiently to block the rectifier, CR_2. In any case, The fall of I_0 is gradual and reverse recovery of CR_2 occurs without undue transient power dissipation. This completes the cycle of operation of the resonant switching dc-dc converter.

Each operating cycle of the dc-dc converter is initiated by a trigger pulse as shown in Figure 7. At completion of a cycle, the converter becomes quiescent until the next trigger pulse. The output voltage is controlled by passing regularly occurring trigger pulses through a gate which either allows each pulse through or inhibits it depending on the instantaneous error between the output voltage and a dc reference voltage. This triggering technique is called pulse train regulation.

Figure 8 illustrates pulse train regulation. The magnitude of the ripple voltage due to regulating action on the output of the converter is limited by the hysteresis of the controller. Hysteresis is maintained at a level permitting the peak-to-peak ripple voltage on the dc output to be held to a small fraction of the output voltage. Figure 8 illustrates two extreme cases. For heavy load and low input voltage, most of the trigger pulses are gated to the converter to maintain the output voltage within the required tolerance. For light load and high input voltage, only a few trigger pulses are required.

The resonant switching converter is adapted to make an inverter by adding another secondary winding and rectifier diode on the inductor, L_1, providing a phase switch to activate one rectifier at a time on successive half-cycles of output voltage, and using a sinewave instead of a dc reference voltage. Figure 9 illustrates the basics of a resonant switching inverter.

Q_2 and Q_3 constitute a phase switch driven by phase drive through transformer, T_2, from the controller. The phase switch deactivates CR_5 by means of high impedance in series and activates CR_4 by closing the CR_4 circuit during the positive half-cycle of E_0. Similarly, during the negative half-cycle, CR4 is deactivated and CR5 is activated. The controller includes a high frequency pulse generator, squarewave phase drive generator at the frequency of E_0, sinewave voltage reference, sinewave voltage comparator, and high frequency pulse gate controlled by the comparator. The circuit on the primary side of L_1 is the same as in a dc-dc converter.

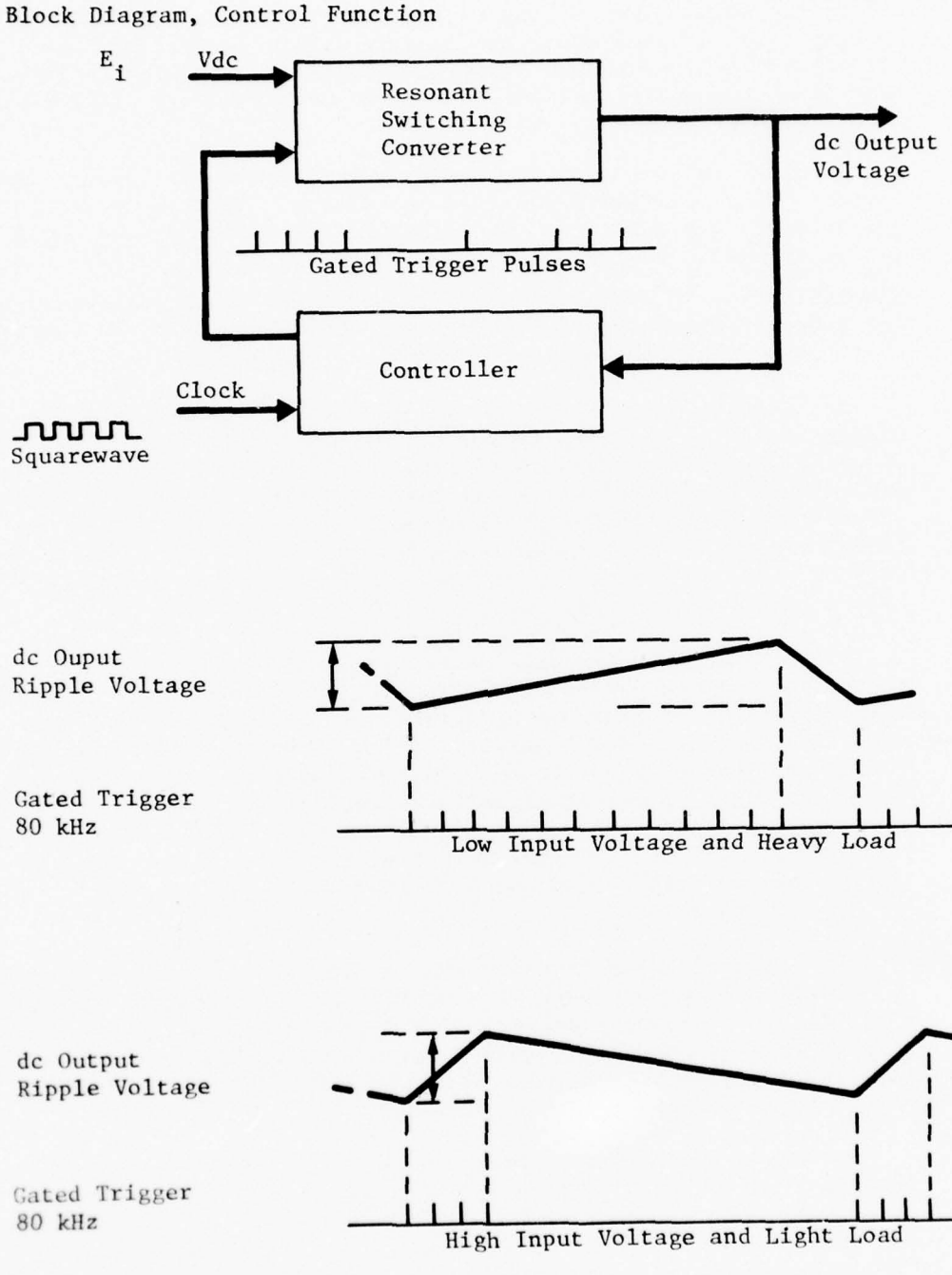

Figure 8. Control function, resonant switching converter.

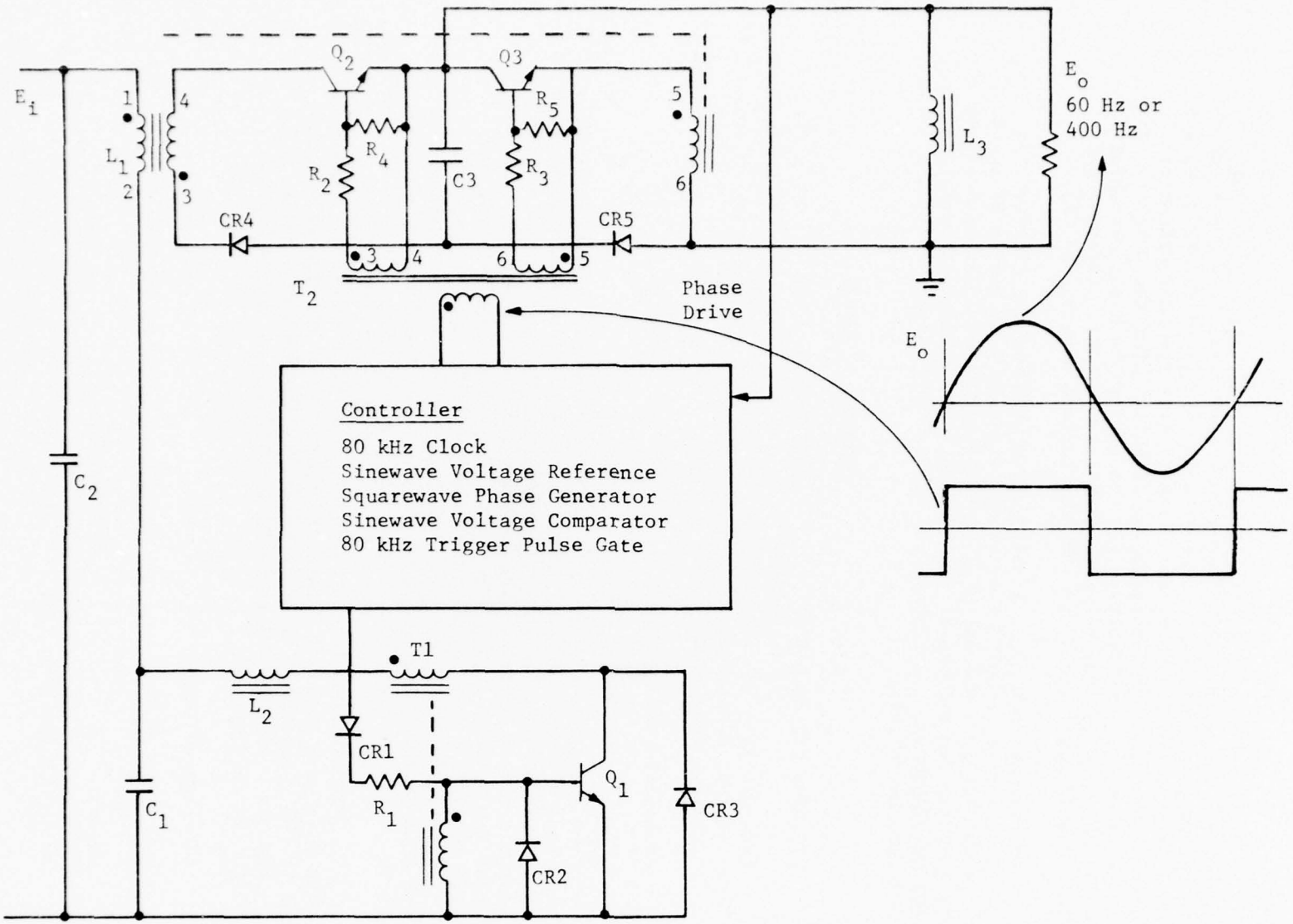

Figure 9. Resonant switching inverter.

Silicon Controlled Rectifier Version of Resonant Switching Inverter. Except for high frequency limitations, SCRs can be used in the resonant switching inverter with SCRs in place of Q_1, Q_2 and Q_3. As shown in Figure 9, the circuit turns the SCRs off as required without special commutating circuits. For the positive half-cycle of E_0, one high-voltage SCR can perform both the switching function of Q_2 and the rectifying function of CR_4. Likewise for the negative half-cycle, one SCR can replace both Q_3 and CR5.

To evaluate the speed limitations of SCRs in the primary side of the inverter circuit, that is Q_1 of Figure 9, a series of tests were made using a 90-watt breadboard operating at a repetition rate of 10 kHz. Two different SCRs were tested: The International Rectifier 92RM30 and the Transitron TC2020. The ratings for these SCRs are as follows:

	92RM30	TC2020
Blocking Voltage, V	300	200
Turn-off time (microsec) for	10	7
-di/dt, A/microsec	5	no spec
dv/dt, V/microsec	200	30
Average forward current, A	95	10

From the test results it is projected that the 92RM30 could be used in a 300-watt circuit; however, the maximum feasible repetition rate would be about 15 kHz. At this rate, 18 would be the maximum possible number of pulses per half-cycle of 400 Hz output. With these few pulses, it would be impossible to achieve suitable voltage regulation due to poor resolution. Filtering to obtain good waveform would likely be heavy. For these reasons the attempt to use SCRs in the primary side of the inverter was abandoned in favor of transistors to complete the investigation.

To evaluate SCRs in the secondary side of the inverter, tests were made on a 100-watt breadboard operating at a repetition rate of 80 kHz. A General Electric Type C144PX22 SCR replaced CR_4 and Q_2 and the same type SCR replaced CR_5 and Q_3. This SCR has the following ratings.

Blocking voltage	900
Turn-off time	20 microsec
dv/dt	200V/microsec
Average forward current	20A

The results showed that at 80 kHz, with peak currents of 10 amperes, these SCRs do not turn off reliably and are inefficient. The main problem besides turn-off time appears to be insufficient di/dt rating at turn-on. It was projected that to obtain adequate performance, the repetition rate would have to be reduced to 20 or 30 kHz maximum. Another difficulty in using SCRs as combined phase switches and SCRs in the circuit of Figure 9, is that the positive voltage drive from T_2 remains on the SCR gates during reverse blocking periods. Reverse blocking capability with positive gate drive is not specified and is probably greatly reduced below normal reverse voltage capability. To overcome this problem, a revised phase drive would be needed to remove positive gate voltage during reverse blocking periods. For these reasons it was decided to revert to transistors and diodes in the secondary side and the primary side to complete the investigation.

Transistorized Inverter. The transistors chosen to evaluate resonant switching techniques are RCA 2N6032 for the primary side and Solitron SDT96306 for the secondary side. Figure 9 shows a single transistor, Q_2 or Q_3, for each half cycle of E_0. For E_0 = 120 Vrms and E_i = 60 Vdc, the voltage applied to Q_2 or Q_4 may be over 800 volts. The Solitron SDT96306 is rated at V_{CBO} = 325V and V_{CEO} = 300V. Until higher voltage-rated transistors could be obtained with sufficient speed to operate at 80 kHz, it was necessary to divide the voltage among three SDT96306s for each half of the secondary. This arrangement gives reliable operation for evaluation purposes for E_i = 30 to 60 volts and E_0 = 120 Vrms.

Final Design - Transistorized Resonant Switching Inverter

A block diagram of the 60 Hz, 400 Hz sinewave inverter is shown in Figure 10. Input power is processed in the power switch assemblies without preregulation. The basic approach involves three phases, identical in configuration, each having a total volt-ampere capability of 1500 VA. Normal steady-state, full load capability is 1000 watts per phase. The additional VA capability will accommodate 20 percent overload simultaneous with a 0.8 load power factor.

Each phase consists of five identical 300 VA power stage assemblies operating in parallel. Each phase has an output filter, a sinewave controller, a phase switch drive amplifier, and an overcurrent sense element.

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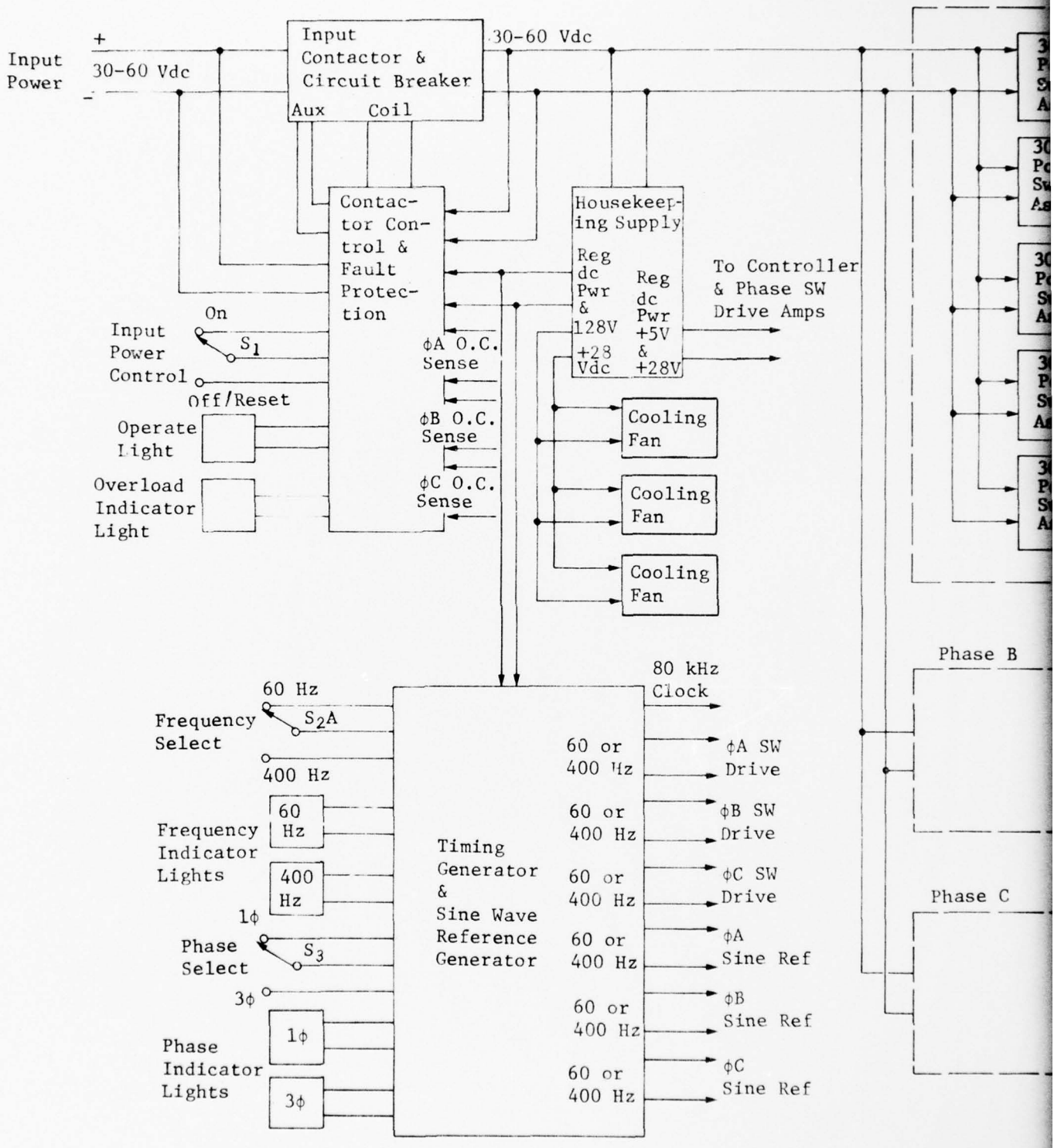
Input Power
+
30-60 Vdc
-
Input Contactor & Circuit Breaker
Aux
Coil
30-60 Vdc
Contactor Control & Fault Protection
Housekeeping Supply
Reg dc Pwr & 128V
Reg dc Pwr +5V & +28V
+28 Vdc
To Controller & Phase SW Drive Amps
On
Input Power Control
S1
Off/Reset
Operate Light
Overload Indicator Light
φA O.C. Sense
φB O.C. Sense
φC O.C. Sense
Cooling Fan
Cooling Fan
Cooling Fan
Phase B
Phase C
60 Hz
Frequency Select
S2A
400 Hz
Frequency Indicator Lights
60 Hz
400 Hz
1φ
Phase Select
S3
3φ
Phase Indicator Lights
1φ
3φ
80 kHz Clock
Timing Generator & Sine Wave Reference Generator
60 or 400 Hz
φA SW Drive
60 or 400 Hz
φB SW Drive
60 or 400 Hz
φC SW Drive
60 or 400 Hz
φA Sine Ref
60 or 400 Hz
φB Sine Ref
60 or 400 Hz
φC Sine Ref

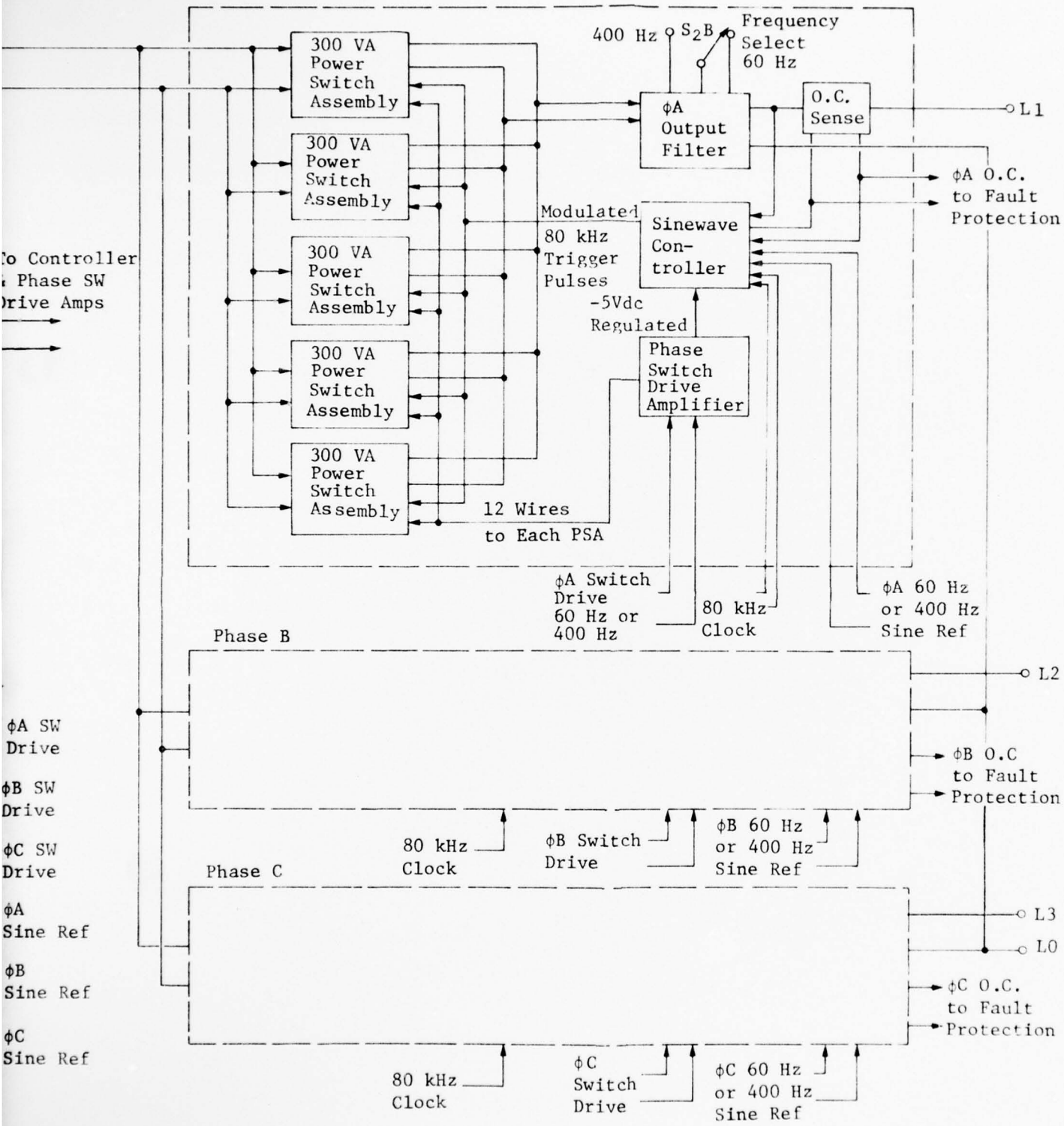

Figure 10. SLEEPS Inverter Block Diagram.

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Input Contactor. A modified Hartman type A-885 has been chosen for the SLEEPS 3 kW inverter. This contactor is a DPST momentary type unit with contacts connected in parallel to give 200 ampere SPST capability. The contactor also has SPST auxiliary contacts. Modifications include an economizer coil to reduce power dissipation during operation, and an overcurrent protection without additional circuitry.

A momentary type contactor was chosen rather than a magnetic latching type because of the simplicity of implementing reverse voltage protection using this type unit.

Housekeeping Supply. Figure 11 shows a schematic diagram depicting the basic approach to the housekeeping supply. The circuit chosen is a conventional switching regulator with 30 to 60 Vdc input from the load side of the contactor, and a regulated 28 Vdc output. Regulated 28 Vdc is supplied to the fault protection circuits and to the cooling fans which are brushless dc fans with built-in solid-state inverters. An additional regulator is incorporated to supply +5 Vdc to the timing generator, sinewave reference generator, and to the fault protection circuits. The -5 Vdc required for the sinewave controller is derived from the phase switch drive amplifier.

Timing Generator and Sinewave Reference Generator. The timing generator diagram is shown in Figure 12. For 400 Hz operation the, 76.80 kHz clock is divided down to 2400 Hz by U1, U2, and U5. It is then applied to a three-phase, squarewave generator consisting of U6, U7, and U8. The resulting 400 Hz, three-phase squarewaves are used to drive the phase switch drive amplifiers of each phase. For 60 Hz operation, the clock frequency is changed to 80.64 kHz and an additional divide by seven circuit is switched in to provide 360 Hz to the three-phase, squarewave generator.

The three phases and their complements are available from the timing generator so that any two phases can be operated 180° out of phase for 240 volt, single-phase output.

A low distortion wave for each phase is also available from the circuit of Figure 12. The three low distortion waves are fed to the sinewave reference generator of Figure 13. Here the positive and negative signals for each phase are summed and filtered in bandpass active filters to provide the three sinewave reference signals required by the sinewave controllers of each phase.

The system clock which is not included in Figure 12 would be a part of the timing generator. The clock output of 76.80 kHz or 80.64 kHz is also supplied to the sinewave controller to provide the basic repetititon rate for triggering the power stages.

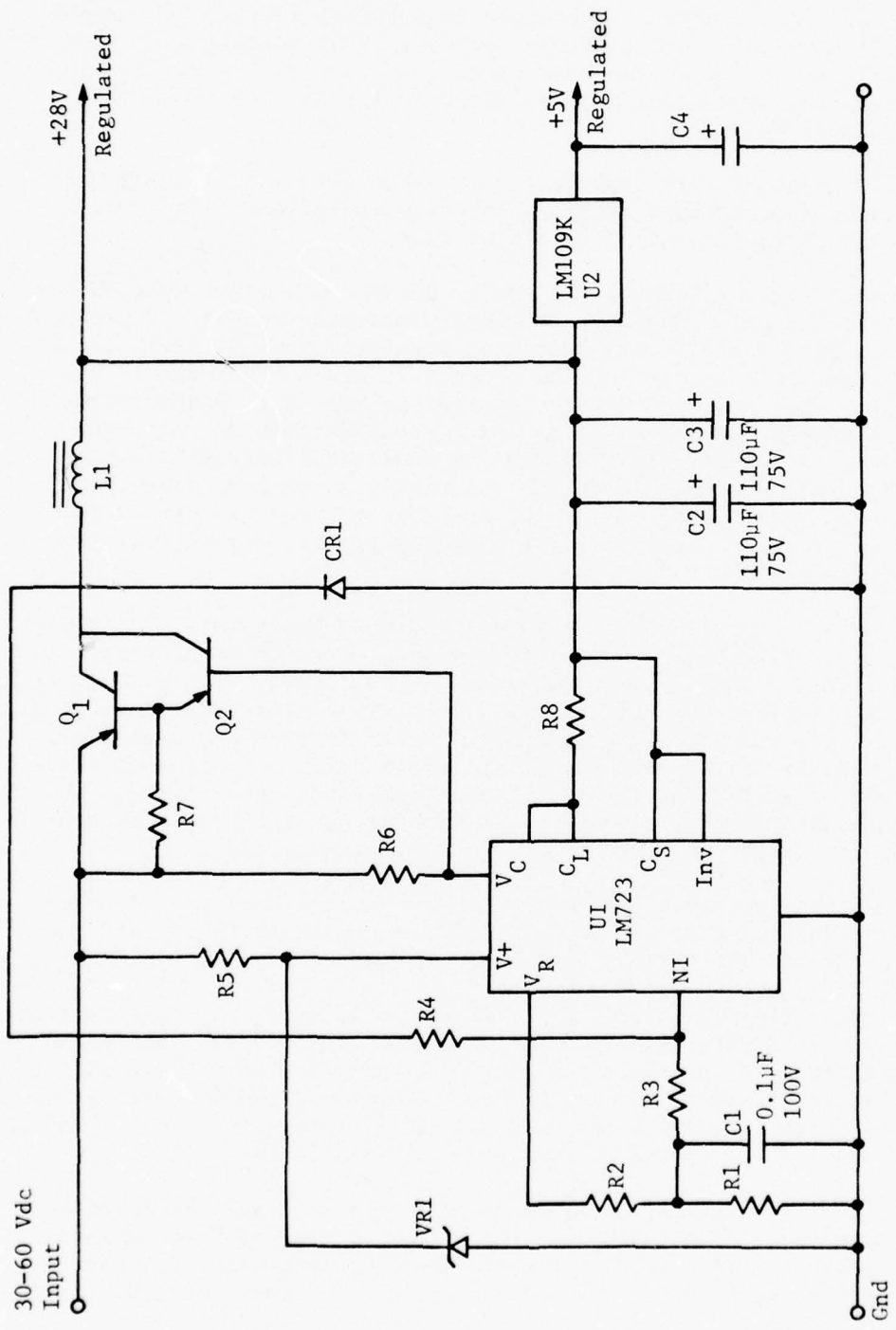
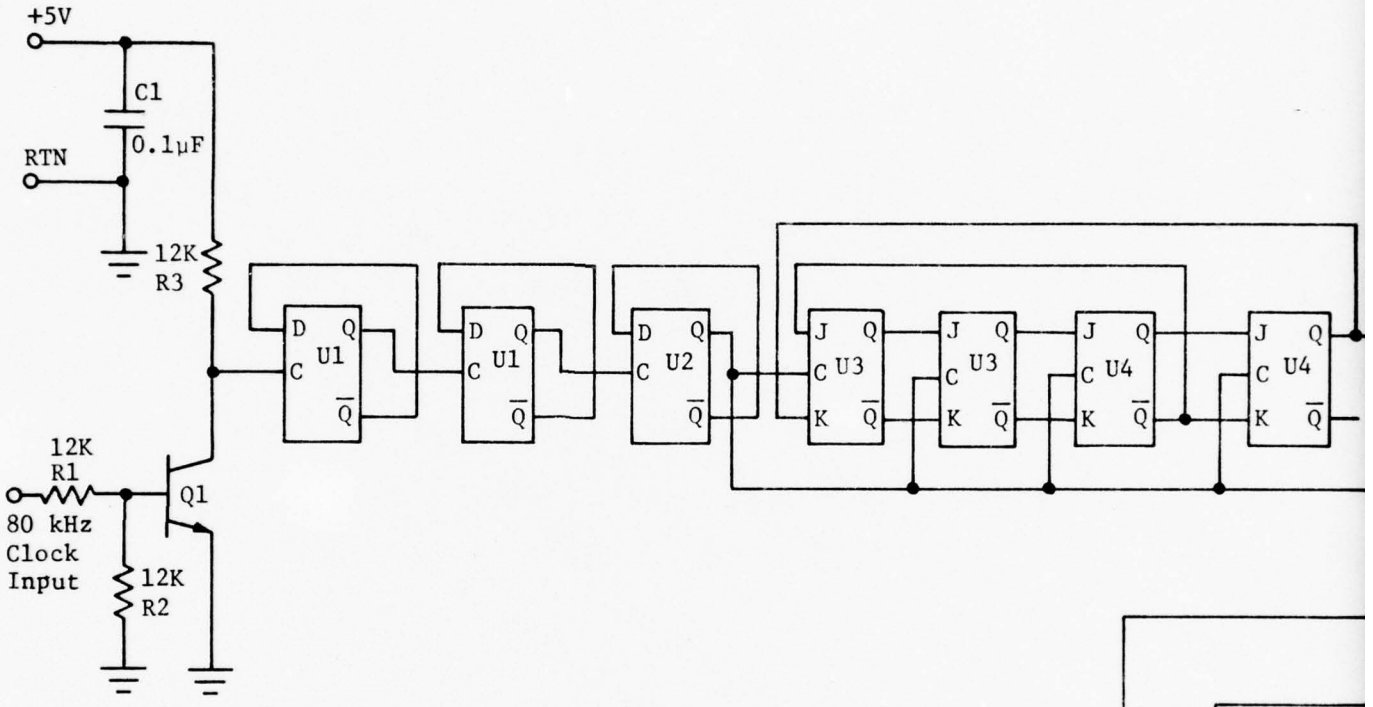
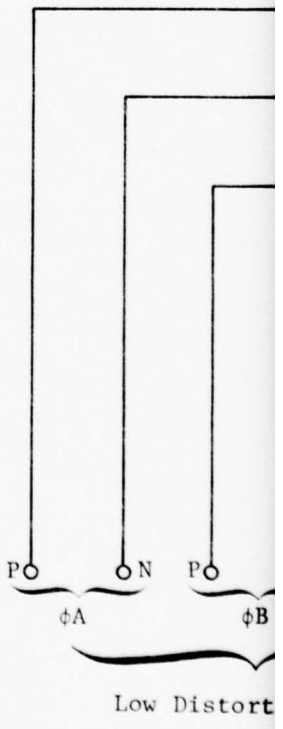


Figure 11. Housekeeping supply.


+5V
C1
0.1μF
RTN
12K
R3
12K
R1
80 kHz
Clock
Input
Q1
12K
R2
D Q
C U1
Q
D Q
C U1
Q
D Q
C U2
Q
J Q
C U3
K Q
J Q
C U3
K Q
J Q
C U4
K Q
J Q
C U4
K Q


P
N
P
φA
φB

Low Distort

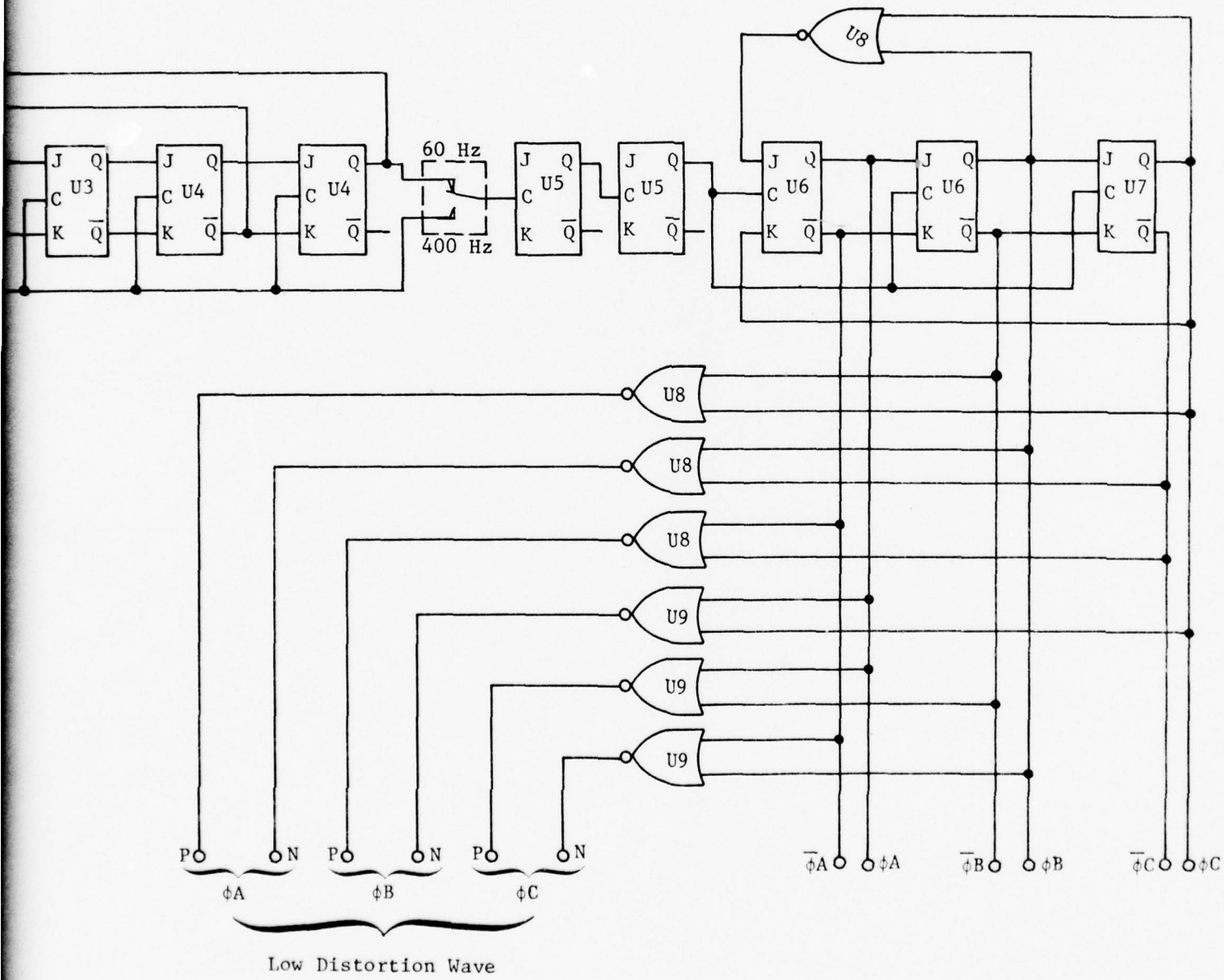


Figure 12. Timing generator.

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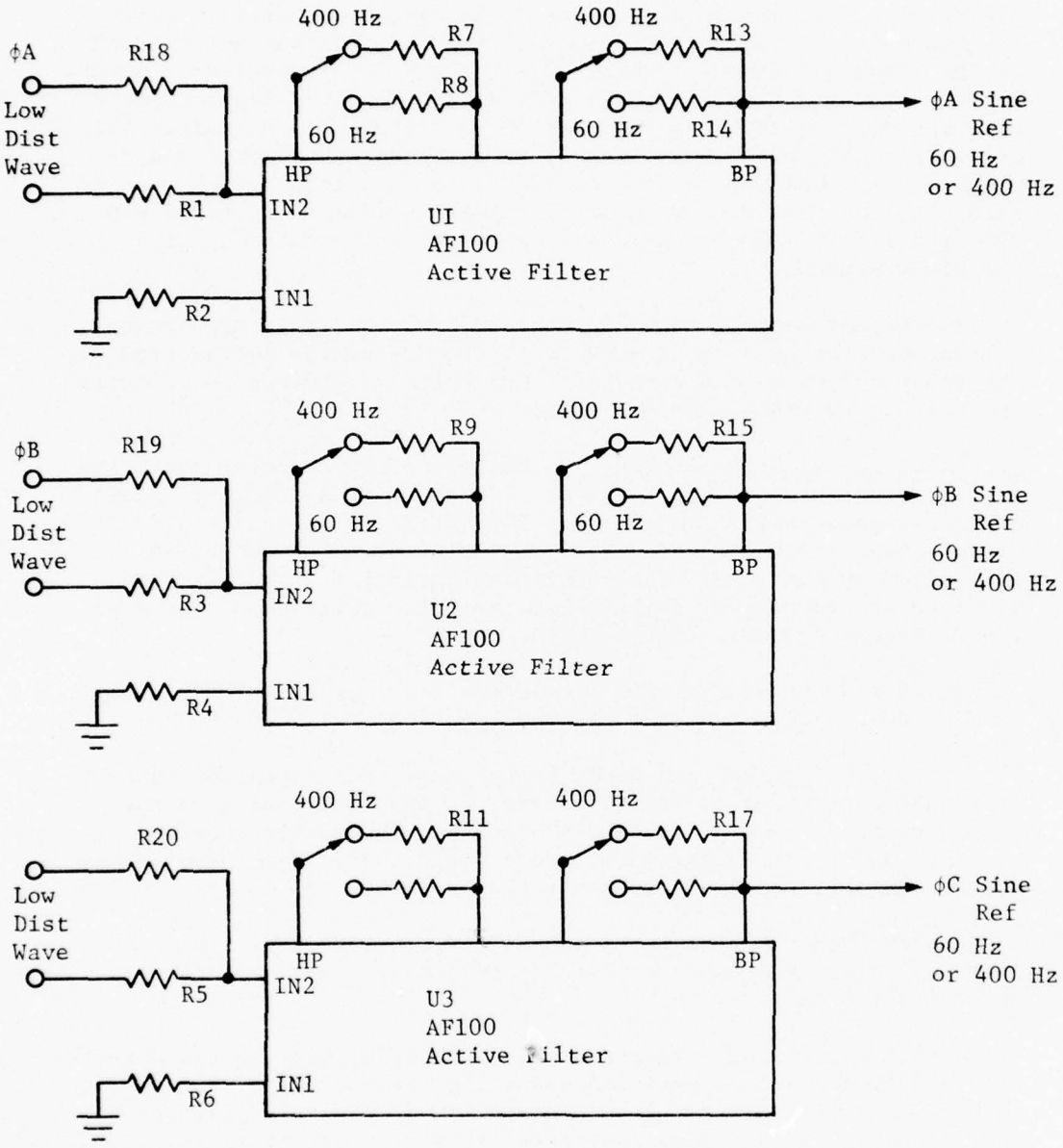


Figure 13. Sinewave reference generator.

Sinewave Controller. The sinewave controllers sense the output waveforms of their respective stages and compare those outputs to the three reference sinewaves provided by the sinewave reference generator. A schematic diagram of a sinewave controller is shown in Figure 14. Comparator U1 compares the inverter output waveform to the reference sinewave while U2 acts as a zero-crossing-detector. Inverters U3 and "AND" gates U4 provide the required logic to make circuits perform as an absolute amplitude comparison circuit. This causes trigger pulses to be issued to the associated power stage whenever the amplitude of the divided down, fed back output wave is less than the reference waveform. Pulse amplifiers Q1 and Q2 provide the 1.5 microsecond pulses required to initiate conduction of the power stages.

The output wave is thus synthesized by pulse train modulation of the power stage at an 80-kHz rate. Pulses are delivered from the power stages to the output filters only as required to maintain the correct waveshape and amplitude.

Phase Switch Drive Amplifier. One phase switch drive amplifier is required for each output phase. Figure 15 is a schematic diagram of a phase switch amplifier. The amplifier is essentially a driven power inverter, capable of operating at 60 or 400 Hz as determined by the input from the timing generator. The six output windings are capable of driving all the phase switches of the five power stage assemblies in one phase.

An auxiliary winding with rectifiers and a filter provide the -5 Vdc power required by the sinewave controller.

Contractor Control and Fault Protection. The contactor control and fault protection circuits provide the capability of inverter on/off control, reverse voltage protection, output overcurrent protection, and input over/under voltage protection. Input overcurrent protection is inherent in the contactor chosen.

Reverse voltage protection for all circuits powered from the output side of the contactor, is achieved by employing a diode in the contactor coil.

Output overcurrent protection is achieved by sensing the current at the output of each phase and using the current signal for two purposes: (1) to limit the modulation by reducing sinewave reference level in the sinewave controller (the circuitry to accomplish this limiting has not been designed but would be incorporated into the sinewave controller circuits), and (2) to shutdown the inverter by opening the contactor if the overcurrent is severe or sustained. The shutdown would be controlled by comparing output current to two fixed references. For severe overcurrents no time delay would be employed. For moderate overcurrents a time delay would be used.

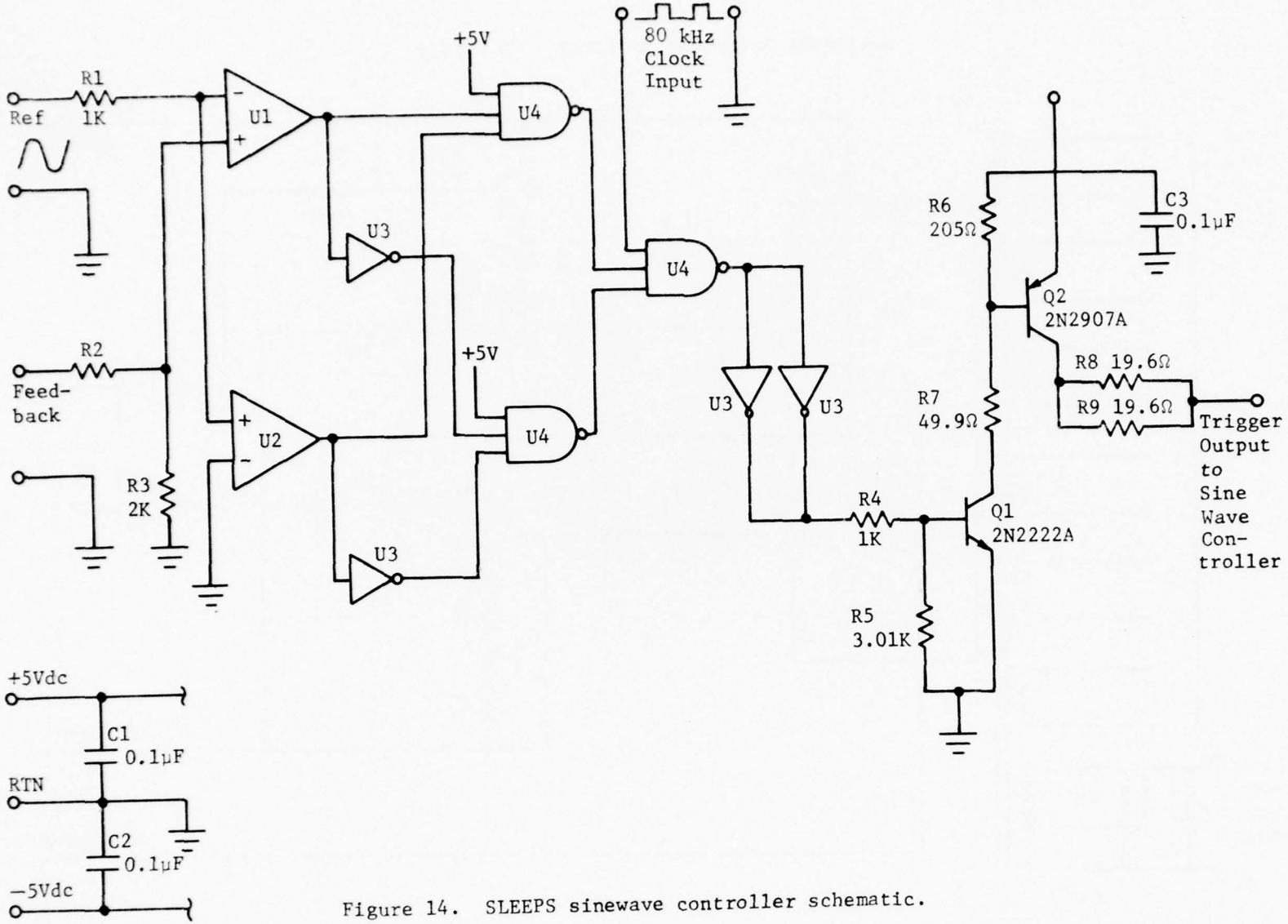


Figure 14. SLEEPS sinewave controller schematic.

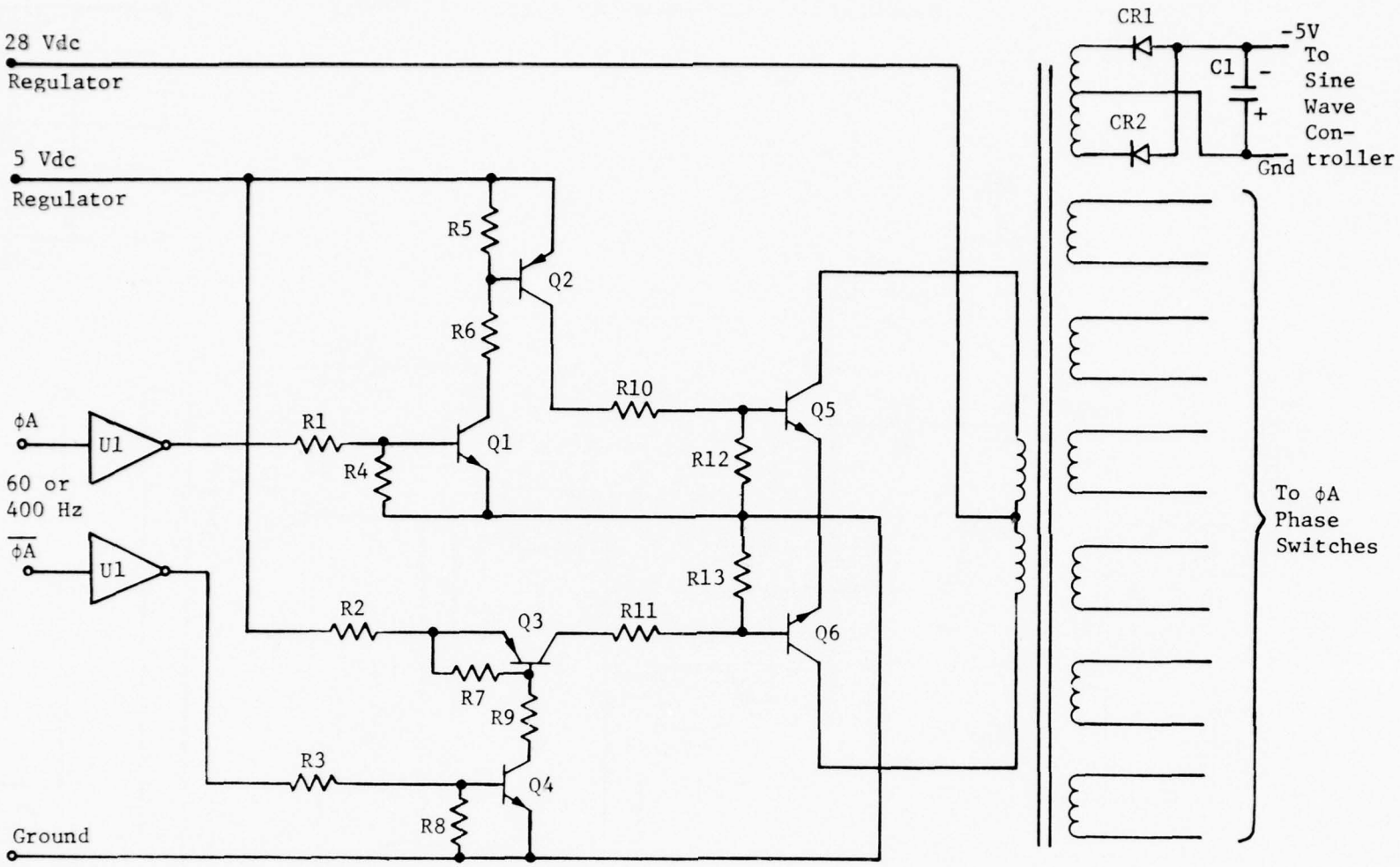


Figure 15. Phase switch drive amplifier.

300 VA Power Switch Assembly. Figure 16 shows the circuit of a 300-VA power switch. Three phase switches in each half of the secondary side of L1 are required to support the high voltages present during normal operation. The output filter is not shown in Figure 16 because all five power switches are connected in parallel to one output filter which is a parallel LC filter resonant at the required output frequency, 60 or 400 Hz. Each power switch has its own input filter capacitor, C_7, in Figure 16.

Breadboard Evaluation Testing

Evaluation testing was accomplished on a 100-watt, proof-of-principal breadboard. Figure 17 shows the breadboard test configuration. The breadboard circuits tested included the 100-watt breadboard power stage assembly, the timing generator (without clock), and the sinewave controller. Other elements such as the clock, sinewave reference generator, output filter, housekeeping supply, and phase switch drive amplifier were simulated with laboratory instruments and components.

Since the main emphasis of this phase of the program was on the power stage development and since not all inverter circuits were breadboarded, evaluation tests were selected that would evaluate the circuits that were breadboarded. The following tests were included: (1) line and load regulation, (2) efficiency, (3) total harmonic distortion, (4) single harmonic distortion, (5) dc offset voltage, and (6) transient performance for application and rejection of rated load and transient overload. Where applicable, tests were run with power factors of 1.0 and 0.8.

Test Equipment List. Table 1 lists the equipment used for the breadboard tests.

Regulation, Line, and Load Test Procedure. Output voltage was measured and recorded for all line voltage and load combinations indicated in Table 2, at 60 and 400 Hz.

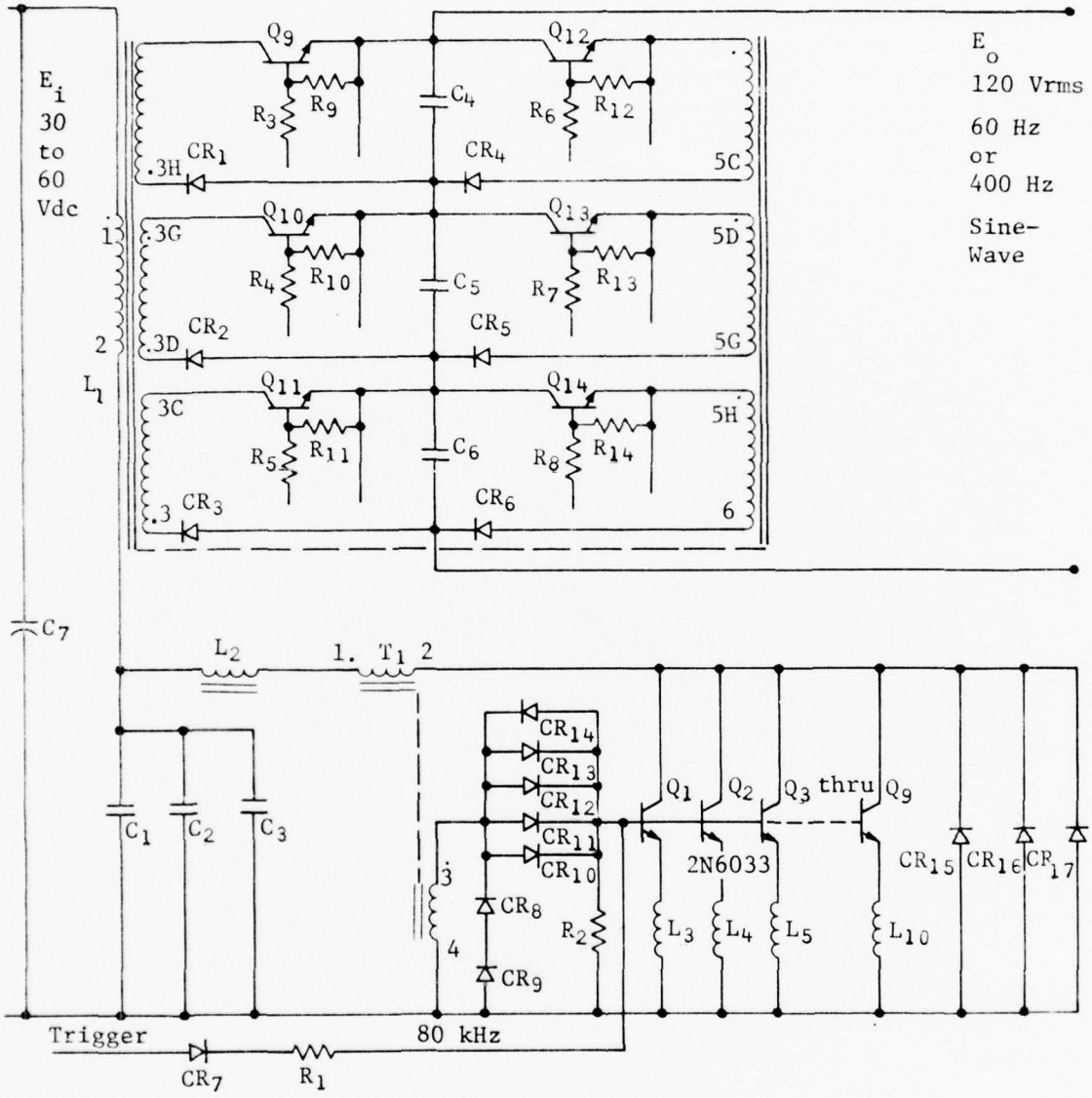


Figure 16. Power switch circuit.

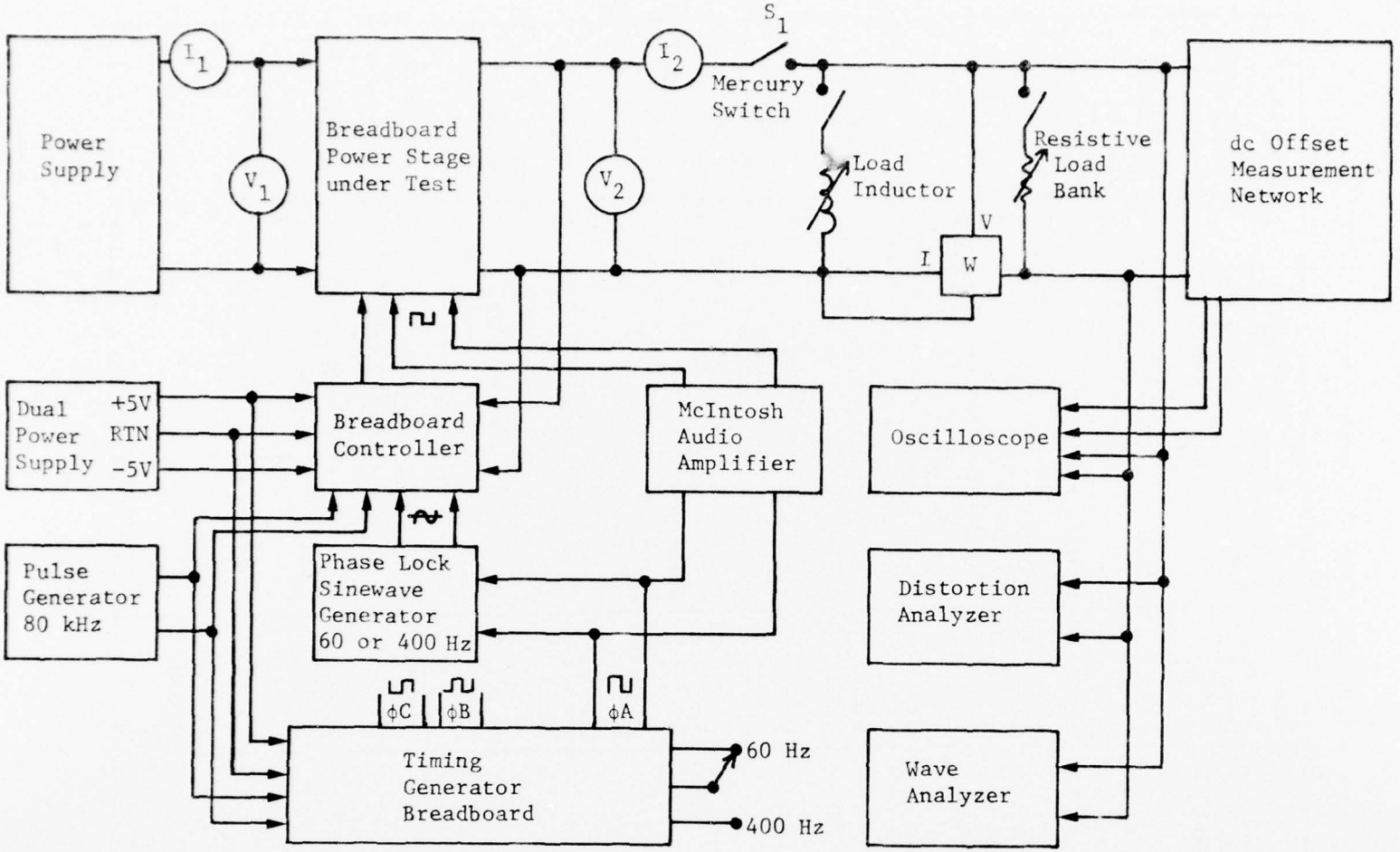


Figure 17. SLEEPS breadboard test configuration.

TABLE 1. TEST EQUIPMENT LIST

Equipment	Mfgr	Model	Description	Equip. No.
Power Supply (Prime Input Power)	Trygon	M7C160-15	0 to 160 Vdc, 15 Amp	EQ534580
Power Supply Dual (Auxiliary Pwr)	HP	6227B	0 to 25V, 0 to 2A each output	ME136901
Pulse Generator (80 kHz clock)	HP	8012A		EQ535515
Function Generator (Reference Sinewave)	HP	3300A		
Phase Lock Plugin	HP	3302A		EQ526186
DVM True RMS (Output Voltage V2)	Fluke	9500A		EQ527001
Distortion Analyzer (Total Harmonic Distortion)	HP	330B		USAF 31571
Wave Analyzer (Single Harmonic Distortion)	HP	302A		USAF 31328
Ammeter (Output Current, I2)	Sensitive Research	RF	0 to 2A	EQ521921
Voltmeter, dc (Input Voltage, V1)	Weston	901	0 to 75 Vdc	ME101272
Ammeter, dc (Input Current, I1)	Weston	901	50 mV, (20A with Shunt)	ME125003
Meter Shunt (Input Current, I1)	Weston		20 Amp - 50 mV	ME125047
Audio Amplifier (Phase Switch Drive)	McIntosh	MC-60		ME104886
Power Meter (Output Power)	Weston	310		ME129950

TABLE 2. TEST CONDITIONS

Condition	Input Voltage, (Vdc)	Load*	Load Inductance, (mH)†	Nominal Load, (volt-amps)	Nominal Load Power, (watts)	Nominal PF
1	30	No load		0	0	1.0
2	30	1/2 load		52	52	1.0
3	30	Full load		104	104	1.0
4	30	1/2 load		65	52	0.8
5	30	Full load		130	104	0.8
6	40	No load		0	0	1.0
7	40	1/2 load		52	52	1.0
8	40	Full load		104	104	1.0
9	40	1/2 load		65	52	0.8
10	40	Full load		130	104	0.8
11	50	No load		0	0	1.0
12	50	1/2 load		52	52	1.0
13	50	Full load		104	104	1.0
14	50	1/2 load		65	52	0.8
15	50	Full load		130	104	0.8
16	60	No load		0	0	1.0
17	60	1/2 load		52	52	1.0
18	60	Full load		104	104	1.0
19	60	1/2 load		65	52	0.8
20	60	Full load		130	104	0.8

*Parallel Load Inductance (Nominal Values)

†Full load 60 Hz - 470 mH
Full load 400 Hz - 74 mH
Half load 60 Hz - 980 mH
Half load 400 Hz - 148 mH

Efficiency Test Procedure. Efficiency was measured and recorded for all input voltage and load conditions indicated in Table 2. The input power was recorded for no-load conditions. Efficiency was measured and recorded at both 60 and 400 Hz.

Total Harmonic Distortion Test Procedure. Total harmonic distortion was measured and recorded for all input voltage and load conditions indicated in Table 2 for both 60 and 400 Hz.

Single Harmonic Distortion Test Procedure. Single harmonic distortion was measured and recorded for conditions 3, 5, 8, 10, 13, 15, 18 and 20 of Table 2 for 400 Hz and for conditions 3, 5, 10, 15 and 18 plus condition 13 at E_i = 45 Vdc for 60 Hz. The second harmonic through the twelfth harmonic were measured for each operating condition listed above.

dc Voltage Offset Test Procedure. Direct current (dc) voltage offset was measured and recorded for each of the input voltage and load combinations of Table 2. The measurements were made using the filter network of Figure 18 and an oscilloscope. The network and oscilloscope were connected as shown in Figure 17.

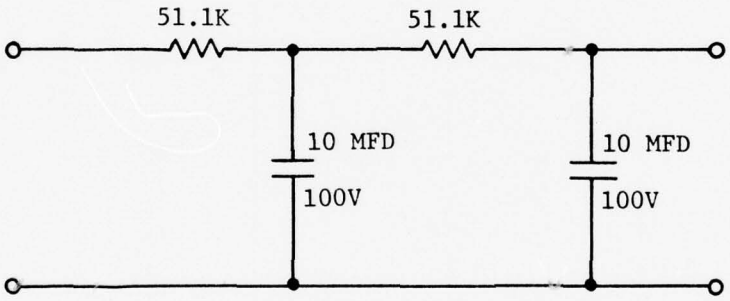


Figure 18. dc offset voltage measurement network.

Application of Rated Load Test Procedure. With the power stage operating steady-state at no load with Vin = 60V, the rated resistive load was applied suddenly by closing load switch S1. The power stage output voltage dip and recovery were monitored by oscilloscope and recorded by photographing the oscilloscope presentation. The test was repeated for rated load at 0.8 power factor.

Rejection of Rated Load Test Procedure. With the power stage operating at full resistive load with Vin = 60V, the load switch was opened. The power stage output voltage rise and recovery were monitored with an oscilloscope and recorded by photographing the oscilloscope presentation. The test was repeated for rated load at 0.8 power factor.

Overload Test Procedure. The power stage was operated at 120% of rated power for 10 seconds minimum, with the input voltage at 40 Vdc. The output voltage, power, and waveform were recorded. The test was repeated with the input voltage at 60 Vdc.

Test Data. The test data for the 100-watt breadboard are given in Tables 3 through 17 and Figures 19 through 24. Tables 3, 4, and 5 cover voltage regulation, efficiency and total harmonic distortion (THD) for 400 Hz. Tables 6, 7, and 8 cover voltage regulation, efficiency and THD for 60 Hz. Single harmonic distortion for 400 Hz is given in Tables 9, 10, 11, and 12, and for 60 Hz in Tables 13, 14, and 15. The results of the 120% overload tests are shown in Tables 16 and 17.

The results of transient load tests for 60 Hz are shown in Figures 19 and 20. In each of these figures the unloaded contact of a single pole, double throw, mercury switch is used as a load switching indicator in the lower trace. This is not an accurate indicator due to a delay between make and break and between break and make.

Figures 21 and 22 show the results of transient load for 400 Hz. In each of these photos, load switching is indicated by load current shown in the lower trace.

Figures 23 and 24 show waveforms for the 120% overload tests for both 60 Hz and 400 Hz operation.

Packaging Design Approach

The prototype design layout shown in Figures 25, 26 and 27 was selected to provide maximum protection and accessibility to the functional subassemblies and to minimize production costs through extensive use of identical modular power units and mechanical details. With the exception of the output filter circuits, contactor, and front panel controls, all circuits are contained in 16 modular chassis arranged in two rows (Figure 26, section B-B). Fifteen of the 16 chassis are identical power switch subassemblies. They are rated at 300VA each and provide the conditioned output power. The 16th module houses the fault protection, sine wave controller, phase switch drive circuits, timing, and housekeeping power supply. The modules are mounted in pairs and inserted vertically in structural guides which engage shear pins at the back of the module chassis. The modules are bolted to the support guide at the forward end. Easily accessible connectors are provided at the forward end of each module.

TABLE 3. REGULATION, EFFICIENCY, WAVEFORM-400 Hz, PF = 1

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	I_o, (Arms)	VA	P_o, (W)	η, (%)*	THD, (%)†	DCO, (mV)§
Full Load	30	5.16	154.8	117.5	0.882	104	105.0	67.8	2.4	75
Full Load	40	4.00	160.0	118.8	0.892	106	107.4	67.1	2.5	110
Full Load	50	3.40	170.0	119.7	0.899	108	108.4	63.8	2.8	120
Full Load	60	3.19	191.4	120.6	0.925	112	110.0	57.5	3.2	130
Half Load	30	3.20	96.0	118.7	0.446	53	54.0	56.3	2.0	60
Half Load	40	2.35	94.0	119.9	0.45	54	55.0	58.5	2.4	85
Half Load	50	1.98	99.0	120.7	0.455	55	55.8	56.4	2.7	95
Half Load	60	1.81	108.6	121.2	0.458	56	56.0	51.6	3.1	120

*η - - - - efficiency

†THD - - - total harmonic distortion

§DCO - - - dc component of output voltage

TABLE 4. REGULATION AND WAVEFORM - 400 Hz, ZERO LOAD

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	THD, (%)	DCO, (mV)
Zero Load	30	0.75	22.5	121.2	2.4	20
Zero Load	40	0.59	23.6	122.0	2.6	22
Zero Load	50	0.48	24.0	122.8	2.8	28
Zero Load	60	0.43	25.8	123.8	3.3	30

TABLE 5. REGULATION, EFFICIENCY, WAVEFORM - 400 Hz, PF = 0.8

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	I_o, (Arms)	VA	P_o, (W)	η, (%)	THD, (%)	DCO, (mV)
Full Load	30	5.38	161.4	118.6	1.144	136	108.4	67.2	2.8	68
Full Load	40	4.14	165.6	119.9	1.160	139	111.0	67.0	3.2	70
Full Load	50	3.45	172.5	121.0	1.170	142	112.6	65.3	3.6	85
Full Load	60	3.30	198.0	122.2	1.183	145	115.0	58.1	3.9	115
Half Load	30	3.07	92.1	119.4	0.560	67	54.6	59.3	2.1	80
Half Load	40	2.39	95.6	120.4	0.565	68	55.8	58.4	2.8	120
Half Load	50	2.00	100.0	121.4	0.572	69	56.2	56.2	3.3	125
Half Load	60	1.83	109.8	121.6	0.575	70	57.4	52.3	3.7	150

TABLE 6. REGULATION, EFFICIENCY, WAVEFORM - 60 Hz, PF = 1.0

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	I_o, (Arms)	VA	P_o, (W)	η, (%)	THD, (5)	DCO, (mV)
Full Load	30	5.25	157.5	117.5	0.897	105.4	106.4	67.6	2.4	160
Full Load	40	4.07	162.8	118.1	0.902	106.5	107.6	66.1	2.3	120
Full Load	50	3.40	170.0	118.1	0.903	106.6	107.8	63.4	2.5	80
Full Load	60	3.35	206.0	119.09	0.91	108.4	109.0	54.2	4.0	120
Half Load	30	3.00	90.0	118.4	0.445	52.7	53.8	58.5	3.5	150
Half Load	40	2.29	91.6	118.6	0.447	53.0	54.0	57.9	3.6	115
Half Load	50	1.93	96.5	119.0	0.445	52.9	54.2	54.9	3.8	80
Half Load	60	1.84	110.4	119.9	0.453	54.3	55.2	49.2	4.4	100

TABLE 7. REGULATION AND WAVEFORM - 60 Hz, ZERO LOAD

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	THD, (%)	DCO, (mV)
Zero Load	30	0.74	22.2	122.4	8.2	110
Zero Load	40	0.57	22.8	122.8	8.4	120
Zero Load	50	0.46	23.0	122.8	8.3	85
Zero Load	60	0.41	24.6	122.9	8.4	50

TABLE 8. REGULATION, EFFICIENCY, WAVEFORM - 60 Hz, PF = 0.8

	E_i, (Vdc)	I_i, (Adc)	P_i, (W)	E_o, (Vrms)	I_o, (Arms)	VA	P_o, (W)	η, (%)	THD, (%)	DCO, (mV)
Full Load	30	5.72	171.6	117.5	1.144	134.4	107.0	62.4	3.8	125
Full Load	40	4.42	176.8	118.3	1.154	136.5	108.0	61.1	3.8	120
Full Load	50	3.74	187.0	118.3	1.156	136.8	108.0	57.8	3.9	80
Full Load	60	3.63	217.8	119.0	1.167	138.9	109.6	50.3	4.4	100
Half Load	30	3.22	96.6	118.5	0.566	67.1	53.6	55.5	3.2	160
Half Load	40	2.43	97.2	118.8	0.568	67.5	53.8	55.3	3.7	160
Half Load	50	2.03	101.5	119.1	0.571	68.0	54.6	53.8	4.1	80
Half Load	60	1.97	118.2	120.2	0.578	69.5	55.4	46.9	4.5	110

TABLE 9. HARMONIC DISTORTION AT 400 Hz, FULL LOAD AND UNITY POWER FACTOR

Harmonic No.	E_{in} = 30 Vdc				E_{in} = 40 Vdc				E_{in} = 50 Vdc			
	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.4	0.16	8.44	2.9	0.35	0.12	7.74	2.8	0.49	0.24	7.84	2.8
3	1.6	2.56			1.70	2.89			1.60	2.56		
4	0.53	0.28			0.55	0.30			0.60	0.36		
5	1.5	2.25			1.30	1.69			1.20	1.44		
6	0.3	0.09			0.40	0.16			0.30	0.09		
7	1.0	1.00			1.10	1.21			1.10	1.21		
8	0.24	0.58			0.17	0.29			0.22	0.05		
9	0.98	0.96			1.00	1.00			1.00	1.00		
10	0.25	0.06			0.19	0.04			0.20	0.04		
11	0.7	0.49			0.09	0.008			0.90	0.81		
12	0.12	0.01			0.20	0.04			0.20	0.04		

TABLE 10. HARMONIC DISTORTION AT 400 Hz, FULL LOAD, UNITY POWER FACTOR AND 60 Vdc INPUT

Harmonic No.	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.58	0.34	10.3	3.21
3	1.9	3.61		
4	0.83	0.69		
5	1.2	1.44		
6	0.48	0.23		
7	1.1	1.21		
8	0.17	0.29		
9	1.2	1.44		
10	0.19	0.04		
11	1.0	1.00		
12	0.13	0.02		

TABLE 11. HARMONIC DISTORTION AT 400 Hz, FULL POWER AND 0.8 POWER FACTOR

Harmonic No.	E_{in} = 30 Vdc				E_{in} = 40 Vdc				E_{in} = 50 Vdc			
	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.34	0.12	4.67	2.2	0.29	0.08	5.40	2.3	0.48	0.23	6.41	2.5
3	1.7	2.89			1.80	3.24			1.90	3.61		
4	0.55	0.30			0.55	0.30			0.55	0.30		
5	0.75	0.56			1.00	1.00			1.10	1.21		
6	0.38	0.14			0.40	0.15			0.57	0.32		
7	0.5	0.25			0.49	0.24			0.48	0.23		
8	0.21	0.04			0.32	0.10			0.49	0.24		
9	0.23	0.05			0.29	0.08			0.18	0.03		
10	0.22	0.05			0.18	0.03			0.24	0.06		
11	0.49	0.24			0.35	0.12			0.37	0.14		
12	0.15	0.02			0.18	0.03			0.18	0.03		

TABLE 12. HARMONIC DISTORTION AT 400 Hz, FULL POWER, 0.8 POWER FACTOR AND 60 Vdc INPUT

Harmonic No.	%	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.85	0.72	10.6	3.26
3	2.4	5.76		
4	0.75	0.56		
5	1.5	2.25		
6	0.55	0.30		
7	0.64	0.41		
8	0.35	0.12		
9	0.40	0.16		
10	0.22	0.05		
11	0.48	0.23		
12	0.20	0.04		

TABLE 13. HARMONIC DISTORTION AT 60 Hz, FULL POWER AND 0.8 POWER FACTOR

Harmonic No.	E_{in} = 30 Vdc				E_{in} = 40 Vdc				E_{in} = 50 Vdc			
	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.3	0.09	10.4	3.2	0.2	0.04	13.8	3.7	0.2	0.04	14.6	3.8
3	2.0	4.00			2.1	4.41			2.3	5.29		
4	0.1	0.01			0.2	0.04			0.15	0.02		
5	1.5	2.25			1.7	2.89			1.9	3.61		
6	0.2	0.04			0.3	0.09			0.3	0.09		
7	1.3	1.69			1.8	3.24			1.7	2.89		
8	0.1	0.01			0.4	0.16			0.1	0.01		
9	1.2	1.44			1.2	1.44			1.2	1.44		
10	0.1	0.01			0.1	0.01			0.1	0.01		
11	0.9	0.81			1.2	1.44			1.1	1.21		
12	0.15	0.02			0.15	0.02						

TABLE 14. HARMONIC DISTORTION AT 60 Hz, FULL POWER AND UNITY POWER FACTOR

Harmonic No.	E_{in} = 30 Vdc				E_{in} = 45 Vdc				E_{in} = 60 Vdc			
	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.05		4.88	2.2	0.05		8.08	2.8	0.4	0.16	11.4	3.4
3	1.6	2.56			1.8	3.24			2.3	5.29		
4	0.05				0.3	0.09			0.1	0.01		
5	0.9	0.81			1.5	2.25			1.8	3.24		
6	0.1	0.01			0.1	0.01			0.1	0.01		
7	0.8	0.64			1.1	1.21			1.1	1.21		
8	0.04				0.03							
9	0.7	0.49			0.8	0.64			1.0	1.0		
10												
11	0.6	0.36			0.8	0.64			0.7	0.49		
12	0.1	0.01										

TABLE 15. HARMONIC DISTORTION AT 60 Hz AND ZERO LOAD

Harmonic No.	E_{in} = 30 Vdc				E_{in} = 45 Vdc				E_{in} = 60 Vdc			
	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$	(%)	$(\%)^2$	$\Sigma(\%)^2$	$\sqrt{\Sigma(\%)^2}$
2	0.4	0.16	76.0	8.7	0.4	0.16	103.8	10.2	0.3	0.09	101.5	10.1
3	5.8	33.6			6.1	37.2			6.0	36.0		
4	0.3	0.09			0.2	0.04			0.2	0.04		
5	4.7	22.1			4.9	24.0			4.9	24.0		
6	0.1	0.01			0.1	0.01			0.15	0.02		
7	2.5	6.25			3.6	13.0			3.3	10.9		
8	0.2	0.04			0.15	0.02			0.1	0.01		
9	2.1	4.41			2.9	8.41			3.0	9.00		
10	0.1	0.01			0.1	0.01			0.2	0.04		
11	2.6	6.76			2.6	6.76			2.5	6.25		
12	0.05	0.003			0.08	0.006			0.1	0.01		
13	2.2	4.84			2.1	4.41			2.2	4.84		
14	0.04	0.002			0.15	0.02			0.2	0.04		
15	1.8	3.24			1.9	3.61			1.9	3.61		
16					0.1	0.01			0.1	0.01		
17	1.5	2.25			1.5	2.25			1.7	2.89		
18												
19	1.2	1.44			1.3	1.69			1.3	1.69		
20												
21	1.0	1.0			1.1	1.21			1.1	1.21		
22									0.05	0.003		
23	1.0	1.0			1.0	1.0			0.9	0.81		

TABLE 16. 120% OVERLOAD TEST - 60 Hz, PF = 1.0

	E_i, (Vdc)	E_o, (Vrms)	P_o, (W)	THD, (%)
100% Load	40	117.9	107.0	3.1
120% Load	40	117.5	130.2	3.1
100% Load	60	119.2	109.0	4.2
120% Load	60	118.9	132.6	4.3

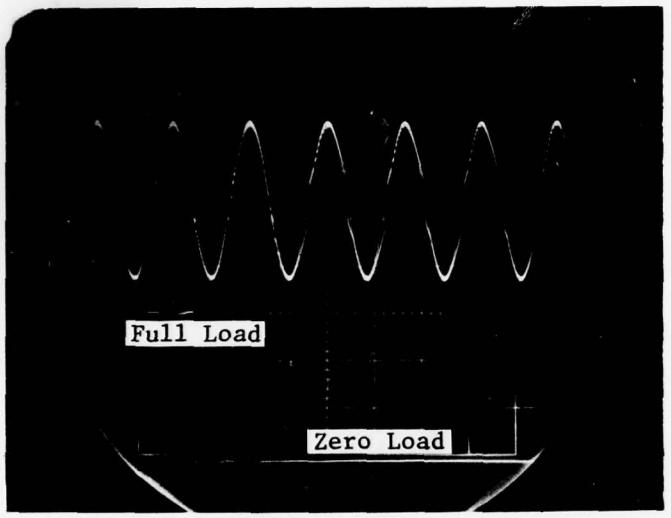
TABLE 17. 120% OVERLOAD TEST - 400 Hz, PF = 1.0

	E_i, (Vdc)	E_o, (Vrms)	P_o, (W)	THD, (%)
100% Load	40	119.0	108.8	2.6
120% Load	40	118.4	130.6	2.7
100% Load	60	120.5	111.8	3.3
120% Load	60	120.2	135.0	3.3

Conditions

E_i = 40 Vdc P_o = 106 W

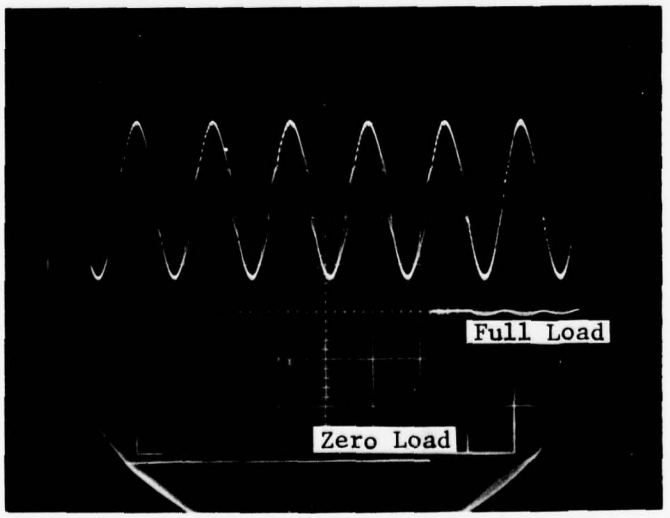
E_o = 119 Vrms



(a) Load Rejection

E_{ref} and E_o (100V/div) Superimposed

(10 msec/div)



(b) Load Acceptance

E_{ref} and E_o (100V/div) Superimposed

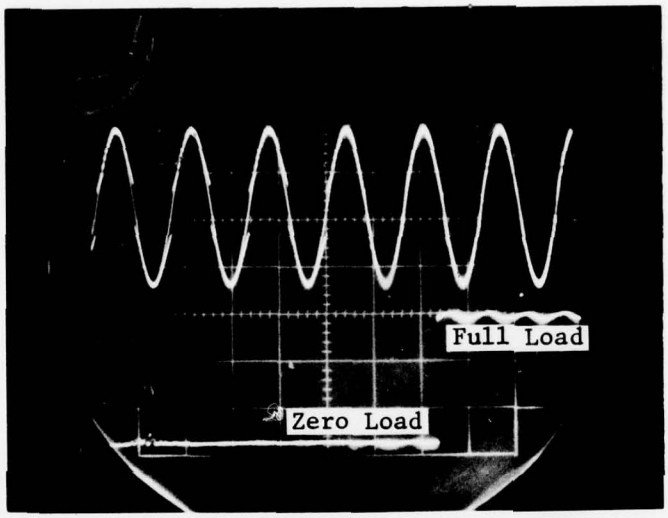
(10 msec/div)

Figure 19. Transient load tests - 60 Hz, 1.0 PF.

Conditions

E_i = 40 Vdc P_o = 106 W

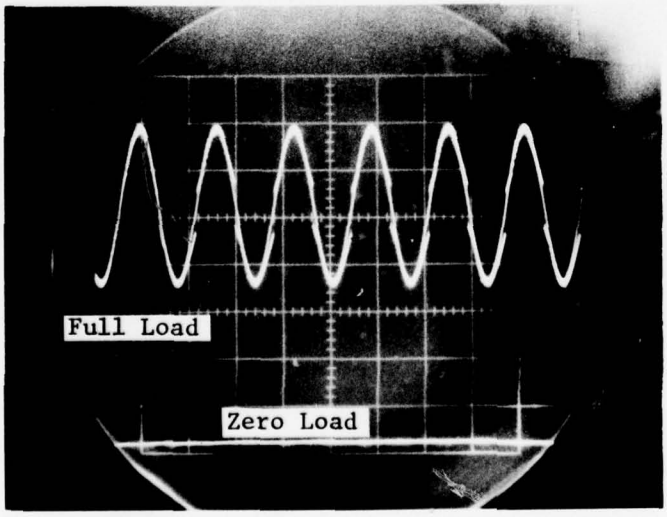
E_o = 119 Vrms



(a) Load Acceptance

E_{ref} and E_o (100V/div) Superimposed

(10 msec/div)



(b) Load Rejection

E_{ref} and E_o (100V/div) Superimposed

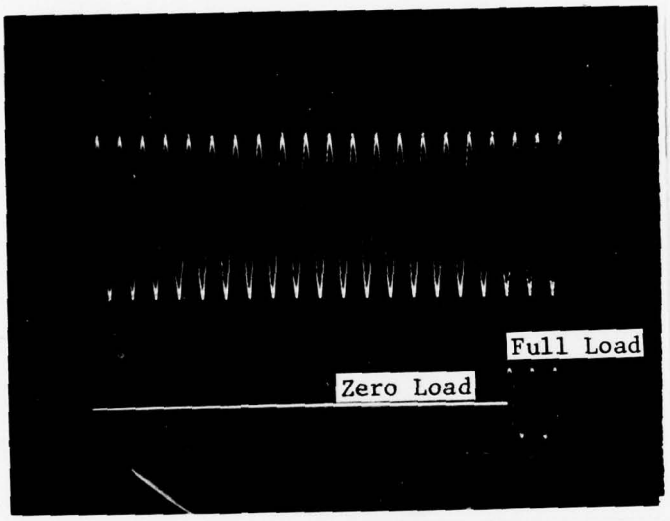
(10 msec/div)

Figure 20. Transient load tests - 60 Hz, 0.8 PF.

Conditions

E_i = 40 Vdc P_o = 106 W

E_o = 119 Vrms

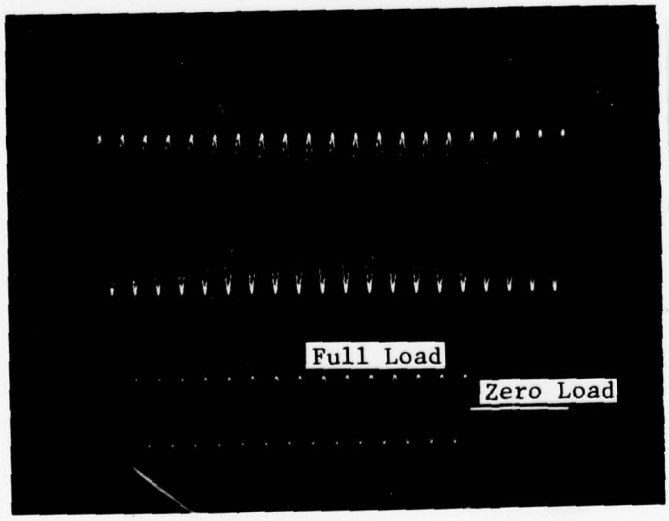


(a) Load Acceptance

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

(5 msec/div)



(b) Load Rejection

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

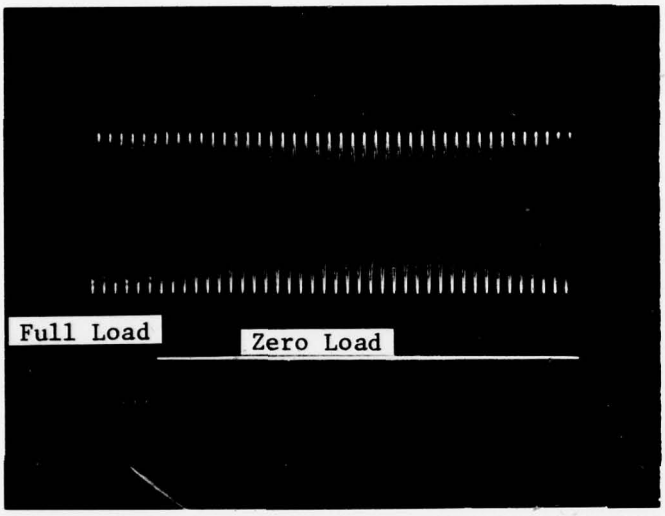
(5 msec/div)

Figure 21. Transient load tests - 400 Hz, 1.0 PF.

Conditions

E_i = 40 Vdc P_o = 106 W

E_o = 119 Vrms

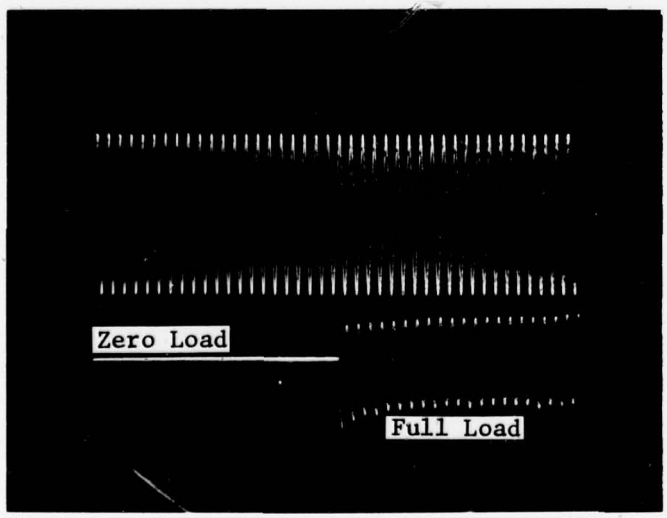


(a) Load Rejection

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

(10 msec/div)



(b) Load Acceptance

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

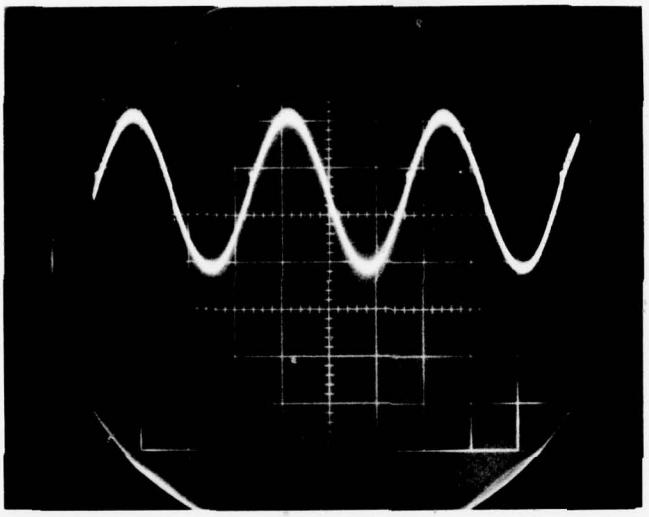
(10 msec/div)

Figure 22. Transient load tests - 400 Hz, 0.8 PF.

Conditions

Full load: $P_o \approx 107.6$ W

$E_o \approx 118.1$ Vrms



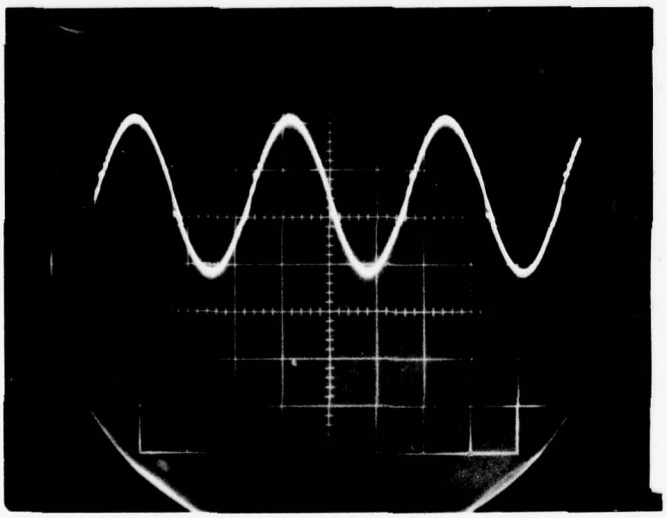
(a) $E_i = 40$ Vdc

$P_o = 130.2$ W

$E_o = 117.5$ Vrms

E_{ref} and E_o (100V/div) Superimposed

(5 msec/div)



(b) $E_i = 60$ Vdc

$P_o = 132.6$ W

$E_o = 118.9$ Vrms

E_{ref} and E_o (100V/div) Superimposed

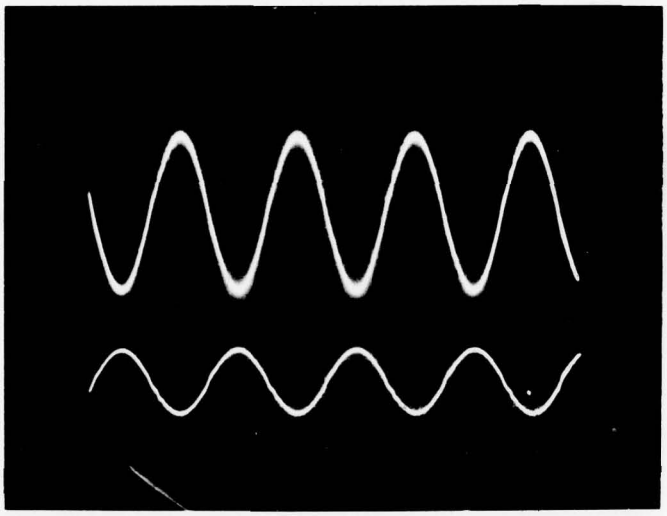
(5 msec/div)

Figure 23. Overload tests - 60 Hz, 120% overload, PF = 1.0.

Conditions

Full load: P_o = 107.6 W

E_o = 118.1 Vrms



(a) E_i = 40 Vdc

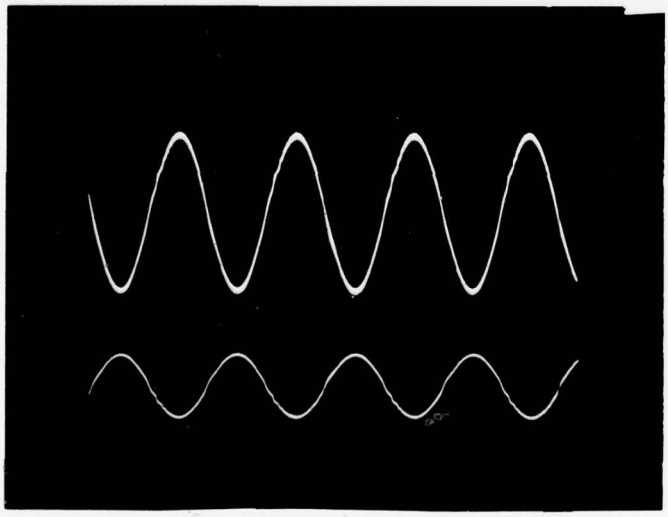
E_o = 119.0 Vrms

P_o = 130.6 W

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

(1 msec/div)



(b) E_i = 60 Vdc

E_o = 120.2 Vrms

P_o = 135 W

E_{ref} and E_o (100V/div) Superimposed

Load Current (2A/div)

(1 msec/div)

Figure 24. Overload tests - 400 Hz, 120% overload, PF = 1.0.

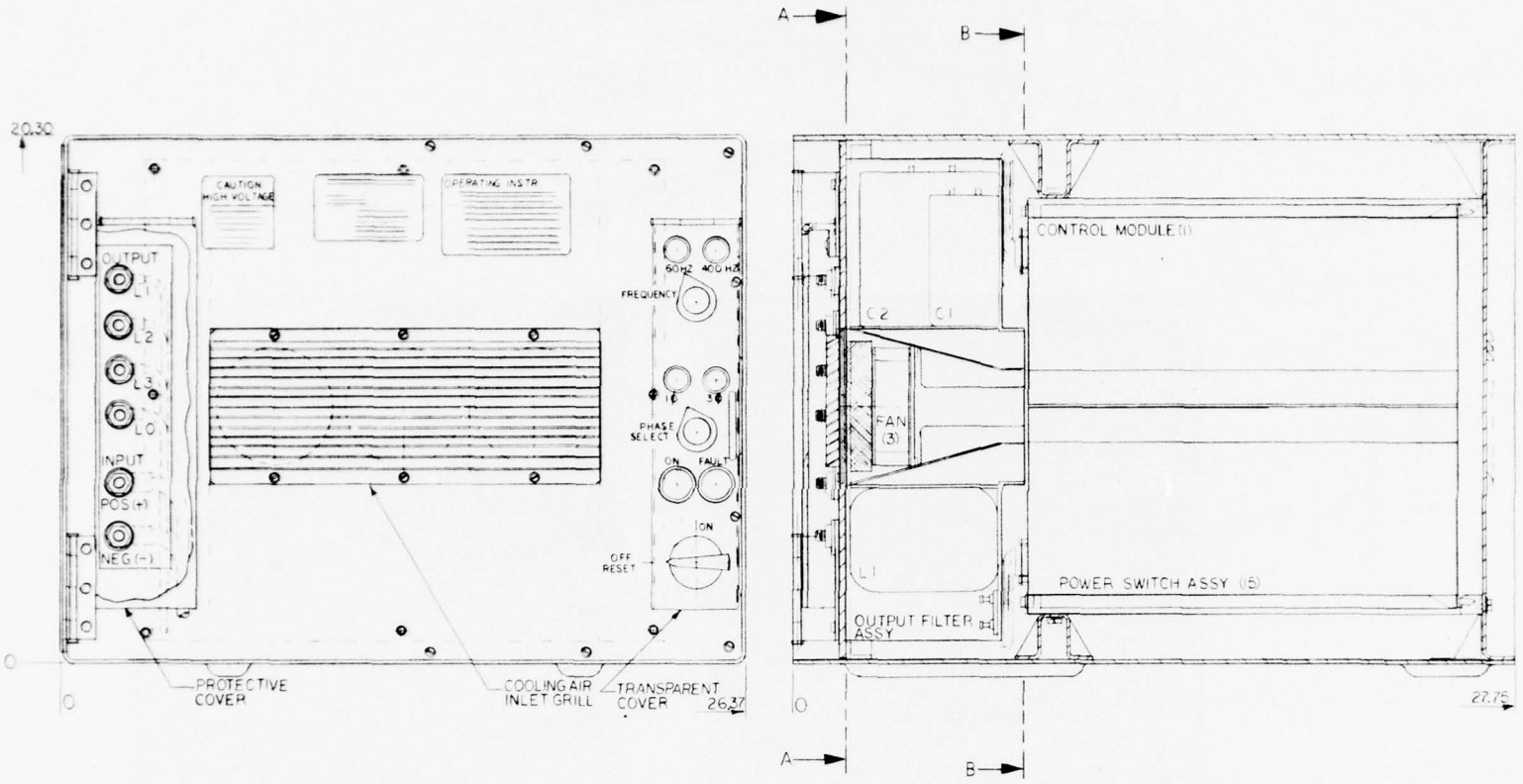


Figure 25. SLEEPS inverter layout.

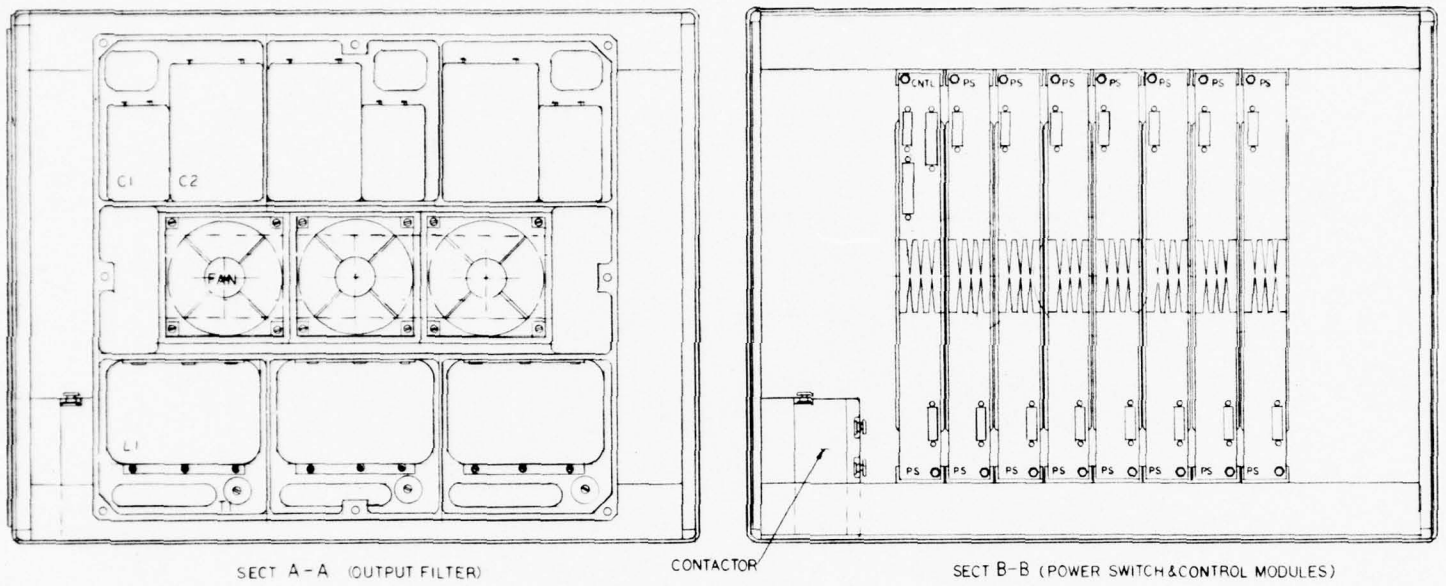


Figure 26. Module arrangement.

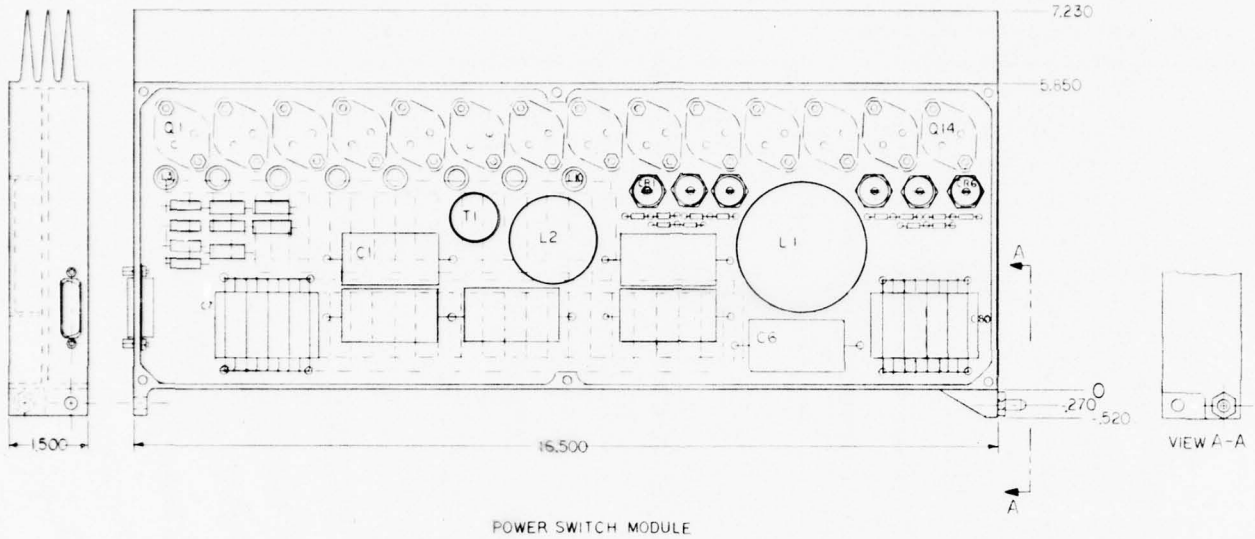


Figure 27. Power switch module.

The output filter circuits are contained in a chassis which is mounted to the back of the front panel. The filter chassis supports the large output chokes and capacitors and an array of three cooling fans centrally located behind the front panel air grill and filter assembly. The output filter chassis incorporates thermal conduction paths and integral fins for heat dissipation.

The main enclosure is formed from 0.090-inch thick aluminum sheet reinforced with structural shapes to support internal loads and provide the desired rigidity. The rear panel with exhaust louvers is rivited at assembly. Sealing flanges are installed to mate with the front panel edges to assure drip proof performance.

The front panel, fabricated from 0.125-inch thick stock is hinged along one side with off-set hinges to allow approximately 180° of opening travel and provide full access to internal modules, associated wiring and front panel-mounted components.

Power Switch Module Design. The 15 power switch modules are packaged as aluminum I-section chassis with integral cooling fins to facilitate forced air cooling. Figure 27 illustrates a proposed parts layout and chassis geometry. The major heat dissipators are arranged close to the fins and are mounted directly to the central chassis wall with individual electrical insulators installed. Since most of the components require chassis mounting for thermal reasons, printed circuit boards are not used. A large number of small tantalum capacitors connected in parallel are mounted on both sides of the central chassis deck. A 25-pin rectangular connector is provided for mating with the internal harness.

Two modules are structurally tied together by lightweight ribbed cover plates. The module pair is supported in the enclosure by shear pins at the rear and fasteners at the front which engage module support guides secured to the enclosure structure.

Control Module Design. The 16th module in the dual row of modules is occupied by the control module. Its construction is similar to the power switch modules, having the same external dimensions and cooling fins but it will be internally compartmented for EMI control. Parts will be mounted on four printed circuit boards supported on machined bosses.

Cooling Provisions. The prototype inverter design used three axial flow fans. They deliver a total of about 135cfm to provide forced air heat transfer from the finned subassemblies. Filtered air from the front panel intake grill is directed past integral fins in the output filter chassis, through the power switch module fins, and is then exhausted through louvers in the rear panel. The straight through flow path and proper sizing of flow passages will assure sufficient mass flow for adequate cooling.

The heat generated in the electrical devices is conducted through the aluminum chassis structure to the fins which are sized to minimize thermal conduction gradients and provide efficient heat transfer to the cooling air.

Maintainability Features. Excellent maintainability is achieved in this prototype design by using modular construction and full accessibility afforded by the hinged front panel. The modules are accessible by opening the front panel, disconnecting the module connector and removing two fasteners located at the forward end of a module pair. Slide-guides assure proper placement and support for the module pair.

Front panel-mounted components are equally accessible due to the wide opening panel facilitating inspection or replacement of components and assemblies.

The air filter which will require periodic maintenance, is directly accessible from the front panel without opening the assembly. The air grill is removed to allow filter maintenance or replacement.

Size and Weight. To adequately support and maintain the prototype inverter in its full range of environments, the package size and weight is found to exceed the design objectives by a significant amount. From the layout the size is 20.30 x 26.37 x 27.75 inches giving a volume of 14,855 in^3 (8.6 cu ft). The weight, summarized below, has been calculated to be 233 pounds. Table 18 is a weight summary of the 3 kW SLEEPS Inverter.

Sleeps Inverter Reliability

Reliability is a measure of the probability of survival of equipment during its mission. The general expression for reliability is

$$R = e^{-\lambda t}$$

where;

R = Reliability, that is the probability of survival

e = exponential (2.71828...)

λ = failure rate in units of failures per hour

t = operating time in hours

TABLE 18. WEIGHT SUMMARY, 3 kW SLEEPS INVERTER

	Weight (lb)
Output switch chassis 15 at 2.35 lb	35.25
Control module chassis	2.85
Output filter chassis	12.40
Module cover tie panels (16)	16.35
Module guides (16)	3.65
Module support rails (16)	4.50
Side stiffeners (4)	2.88
Hinge doubler	0.54
Hinges (2)	0.43
Front panel	6.24
Protective covers (2)	1.13
Panel flanges (3)	0.97
Terminal blocks (2)	0.72
Input/output terminals (6)	0.55
Enclosure	29.00
Fasteners (208)	0.79
Filter, Grill, Wire and Miscellaneous	10.00
Connectors (19)	1.35
Electrical parts	103.40
Total	233.00

The mean time before failure (MTBF) is defined as the reciprocal of the failure rate, That is,

$$MTBF = \frac{1}{\lambda} \tag{2}$$

For the SLEEPS inverter, the required MTBF is 1200 hours. By equation (2) this MTBF is seen to be equivalent to a failure rate of 833×10^{-6} failures per hour.

A reliability model for the SLEEPS inverter is shown in Figure 28. Since the inverter is nonredundant, all blocks are in series and the failure rates of the individual blocks are added to determine the total inverter failure rate. The failure rates of the individual blocks are themselves determined by summing the failure rates of the piece parts internal to the block in accordance with the methods of MIL-HDBK-217B, section 3.0.

For any given block, the failure rate is determined from

$$\lambda_{EQUIP} = \sum_{i=1}^{n} N_i \left(\lambda_G \pi_Q\right)_i \tag{3}$$

for a given environment, where:

λ_{EQUIP} = total equipment failure rate

λ_G = generic failure rate for the i^{th} generic part

π_Q = quality factor for the i^{th} generic part

N_i = = quantity of i^{th} generic part

n = number of different generic part categories

For the SLEEPS inverter analysis, the generic failure rate data applicable for ground mobile environments (Gm in MIL-HDBK-217B) were used. The quality factors applicable to MIL-STD-883, Class B integrated circuits, JAN level transistors and diodes, and established reliability level M capacitors and resistors were used to modify the generic failure rates in accordance with equation 3. The failure rate calculations are summarized in Table 19 for the individual blocks identified in Figure 28. A total failure rate of 673×10^{-6} failures per hour is realized for the SLEEPS inverter. This failure rate is equivalent to an MTBF of 1486 hours.

The detailed breakdown of failure rate calculations for the individual blocks identified in Figure 28 are shown in Tables 20 through 27.

TABLE 19. FAILURE RATE SUMMARY

Block	Failure Rate ($\times 10^{-6}$)
Contractor, Relay, Switches, Fans, Miscellaneous	63.9
Contractor Control/Fault Protection	28.4
Housekeeping Power Supply	5.1
Timing Generator & Sinewave Reference Generator	7.8
Phase A	
Power Switch Assembly	175.6
Output Filter	0.05
Switch Drive Amplifier/Sinewave Controller	13.8
Phase B	
Power Switch Assembly	175.6
Output Filter	0.05
Switch Drive Amplifier/Sinewave Controller	13.8
Phase C	
Power Switch Assembly	175.6
Output Filter	0.05
Switch Drive Amplifier/Sinewave Controller	13.8
Total Failure Rate	673 x 10^{-6}
Inverter MTBF	1486 hr

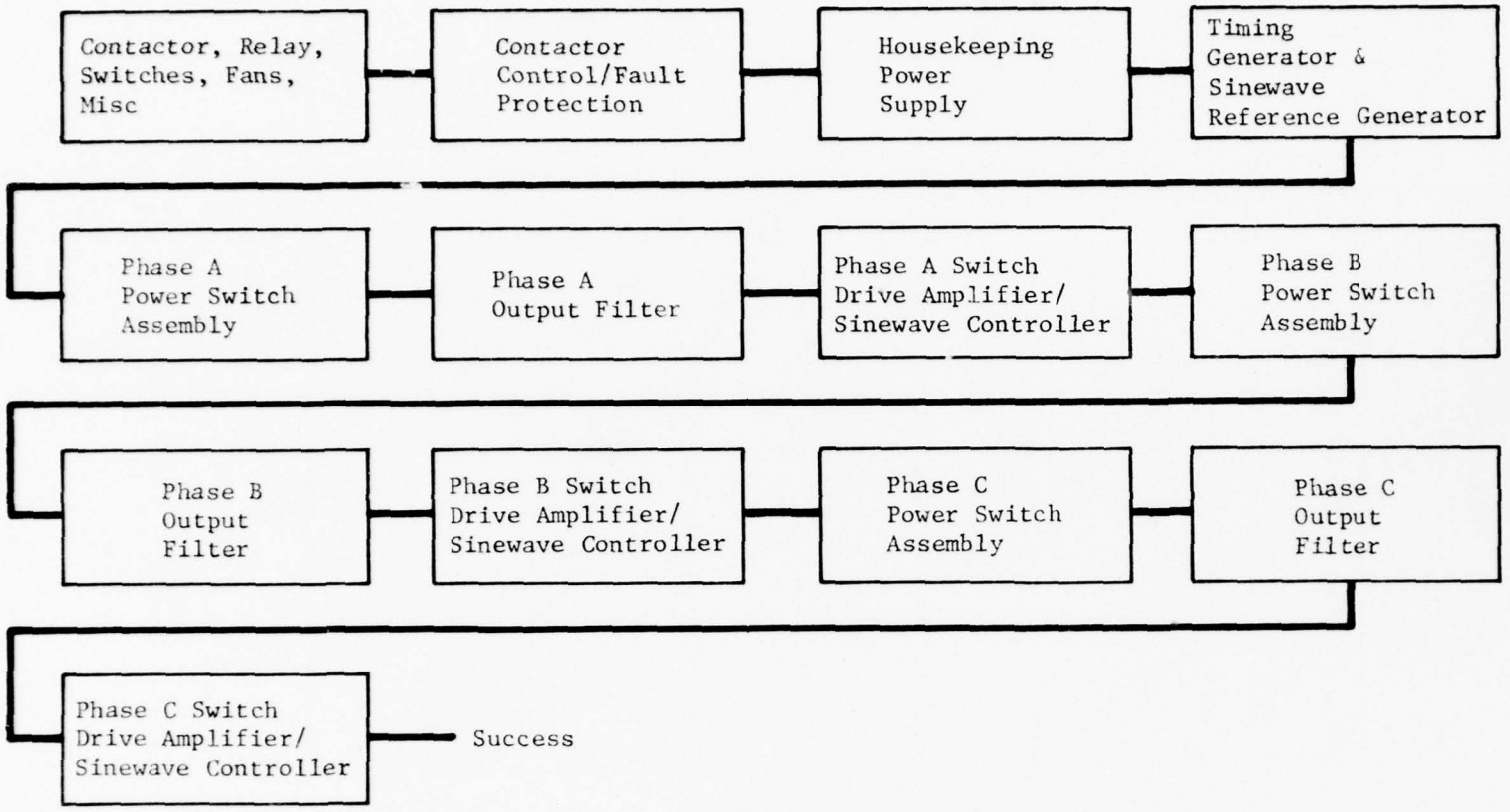


Figure 28. Reliability model.

TABLE 20. CONTACTOR, RELAY, SWITCHES, FANS, MISCELLANEOUS FAILURE RATE

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Connectors			1.0	18	1.0	18
Switches			1.0	3	2.9	8.7
Relays			1.0	1	1.6	1.6
Fans			1.0	3	10.0	30.0
PC Boards			1.0	4	0.0048	0.019
Contactor			1.0	1	5.6	5.6
						63.9

TABLE 21. CONTACTOR CONTROL/FAULT PROTECTION FAILURE RATE

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Film	RNR	M	1.0	117	0.042	4.91
Capacitors						
Ceramic	CKR	M	1.0	19	0.044	0.84
Discrete Semiconductors						
Transistor, Si, FET	2NXXXX	JAN	1.0	6	2.7	16.2
Integrated Circuits						
Linear	--	883B	2.5	19	0.32	6.1
CMOS	--	883B	2.5	1	0.34	0.34
						28.4

TABLE 22. HOUSEKEEPING SUPPLY FAILURE RATE

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Composition	RCN	M	1.0	2	0.0085	0.017
Film	RNR	M	1.0	6	0.042	0.252
Capacitors						
Ceramic	CKR	M	1.0	1	0.044	0.044
Wet Slug	CLR	M	1.0	2	0.11	0.22
Discrete Semiconductors						
Diode, Si, General Purpose	1NXXXX	JAN	1.0	1	0.68	0.68
Transistor, Si, PNP	2NXXXX	JAN	1.0	2	1.60	3.2
Integrated Circuits						
Linear	---	883B	2.5	2	0.32	0.64
						5.1

TABLE 23. TIMING GENERATOR/SINEWAVE REFERENCE GENERATOR FAILURE RATE

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Film	RNR	M	1.0	29	0.042	1.218
Capacitors						
Ceramic	CKR	M	1.0	4	0.044	0.176
Wet Slug	CLR	M	1.0	1	0.11	0.11
Discrete Semiconductors						
Transistor, Si, NPN	2NXXXX	JAN	1.0	2	0.98	1.96
Integrated Circuits						
Linear	---	883B	2.5	4	0.32	1.28
CMOS	---	883B	2.5	9	0.34	3.06
						7.8

TABLE 24. POWER SWITCH ASSEMBLY FAILURE RATE (PER PHASE)

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Wirewound	RWR	M	1.0	14	0.11	1.54
Capacitors						
Wet Slug	CLR	M	1.0	74	0.11	8.14
Plastic	CQR	M	1.0	6	0.0012	0.0072
Discrete Semiconductors						
Diode, Si, General Purpose	1NXXXX	JAN	1.0	17	0.68	11.56
Transistor, Si, NPN	2NXXXX	JAN	1.0	14	0.98	13.72
Magnetics						
Audio XFMR			1.0	10	0.011	0.11
Power XFMR/Filter			1.0	1	0.034	0.034
				Total/Module		35.11
				Total per Phase (X5)		175.6

TABLE 25. OUTPUT FILTER FAILURE RATE (PER PHASE)

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Capacitors						
Plastic	CQR	M	1.0	2	0.0012	0.0024
Magnetics						
Audio XFMR			1.0	1	0.011	0.011
Power XFMR/Filter			1.0	1	0.034	0.034
				Total		0.047

TABLE 26. SWITCH DRIVE AMPLIFIER FAILURE RATE (PER PHASE)

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Film	RNR	M	1.0	13	0.042	0.55
Capacitors						
Wet Slug	CLR	M	1.0	1	0.11	0.11
Discrete Semiconductors						
Diode, Si, General Purpose	1NXXXX	JAN	1.0	2	0.68	1.36
Transistor, Si, NPN	2NXXXX	JAN	1.0	4	0.98	3.92
Transistor, Si, PNP	2NXXXX	JAN	1.0	2	1.60	3.20
Integrated Circuits						
CMOS	--	883B	2.5	1	0.34	0.34
Magnetics						
Audio XFMR			1.0	1	0.011	0.011
				Total per Phase		9.5

TABLE 27. SINEWAVE CONTROLLER FAILURE RATE (PER PHASE)

Description	Part Type	Rel Level	Quality Factor	Qty	λ (x 10^{-6}) Each	λ (x 10^{-6}) Total
Resistors						
Composition	RCR	M	1.0	2	0.0085	0.017
Film	RNR	M	1.0	7	0.042	0.294
Capacitors						
Ceramic	CKR	M	1.0	3	0.044	0.132
Discrete Semiconductors						
Transistor, Si, NPN	2NXXXX	JAN	1.0	1	0.98	0.98
Transistor, Si, PNP	2NXXXX	JAN	1.0	1	1.60	1.60
Integrated Circuits						
Linear	--	883B	2.5	2	0.32	0.64
CMOS	--	883B	2.5	2	0.34	0.64
				Total per Phase		4.3

3. DISCUSSION

The implementation of the resonant switch technique into a 3.0 kilowatt, three phase inverter requires five 300-W modules per phase (see Figure 10). Five modules per phase provide sufficient capability to handle the increased VA load at 0.8 power factors and 120 percent overload. The packaging and reliability studies were made on the basis of five 300-W modules per phase. However, the test data were obtained on a 100-W breadboard. If no further improvements were made, the performance of a full scale inverter can be predicted on the basis of the test results from the 100-W breadboard. The design equations for a 300-W module are the same as for the 100-W breadboard.

Performance

The resonant switching inverter as presently developed and exemplified by the 100-W breadboard shows low efficiency, fair regulations, fair waveform and excellent transient response. These characteristics are all due to high frequency operation. Lower frequency would improve efficiency but would reduce the other three performance characteristics.

The breadboard voltage characteristics are summarized in Figures 29 through 32 as a function of input voltage for various load conditions at 60 and 400 Hz. The SLEEPS regulation requirement of ±2% is met for all conditions except zero load.

Efficiency data obtained on the breadboard unit are summarized in Figures 33 through 36. These data are plotted as a function of input voltage for various load conditions at 60 and 400 Hz. The efficiency obtained is rather poor. The decrease in efficiency at high input voltage is attributable to increased peak currents in both the primary and secondary sides of the resonant switch inverter circuit. These increased currents result in a greater than proportional power loss due to the series resistance of the circuit elements.

At 60 Hz and zero loads the total harmonic distortion is over 8% with individual harmonic content as high 6.1%. For all other conditions, total harmonic distortion is no higher than 4.5%. The third harmonic distortion is 2% or higher under the following conditions at full power:

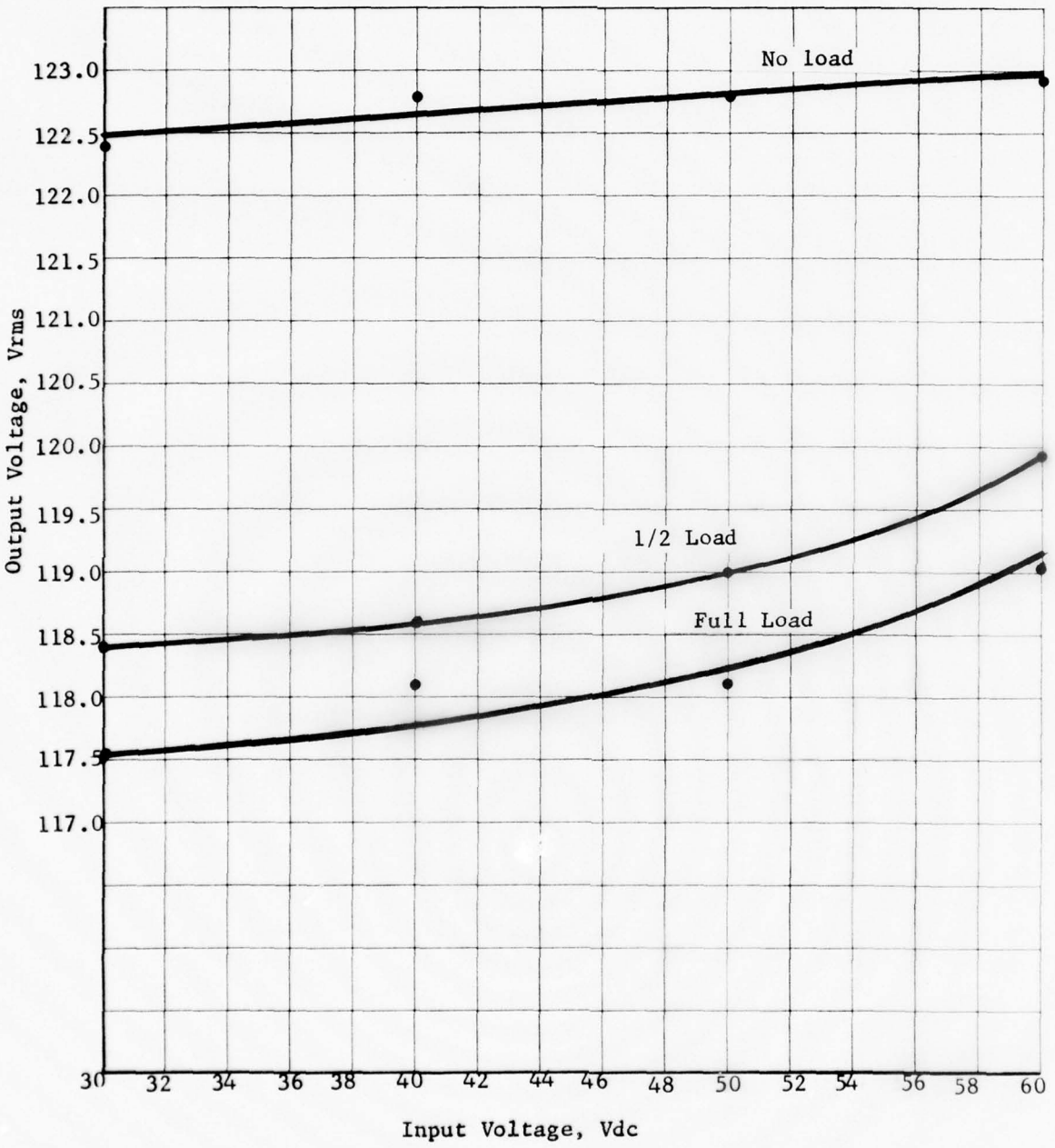


Figure 29. Voltage regulation - 60 Hz, PF = 1.0.

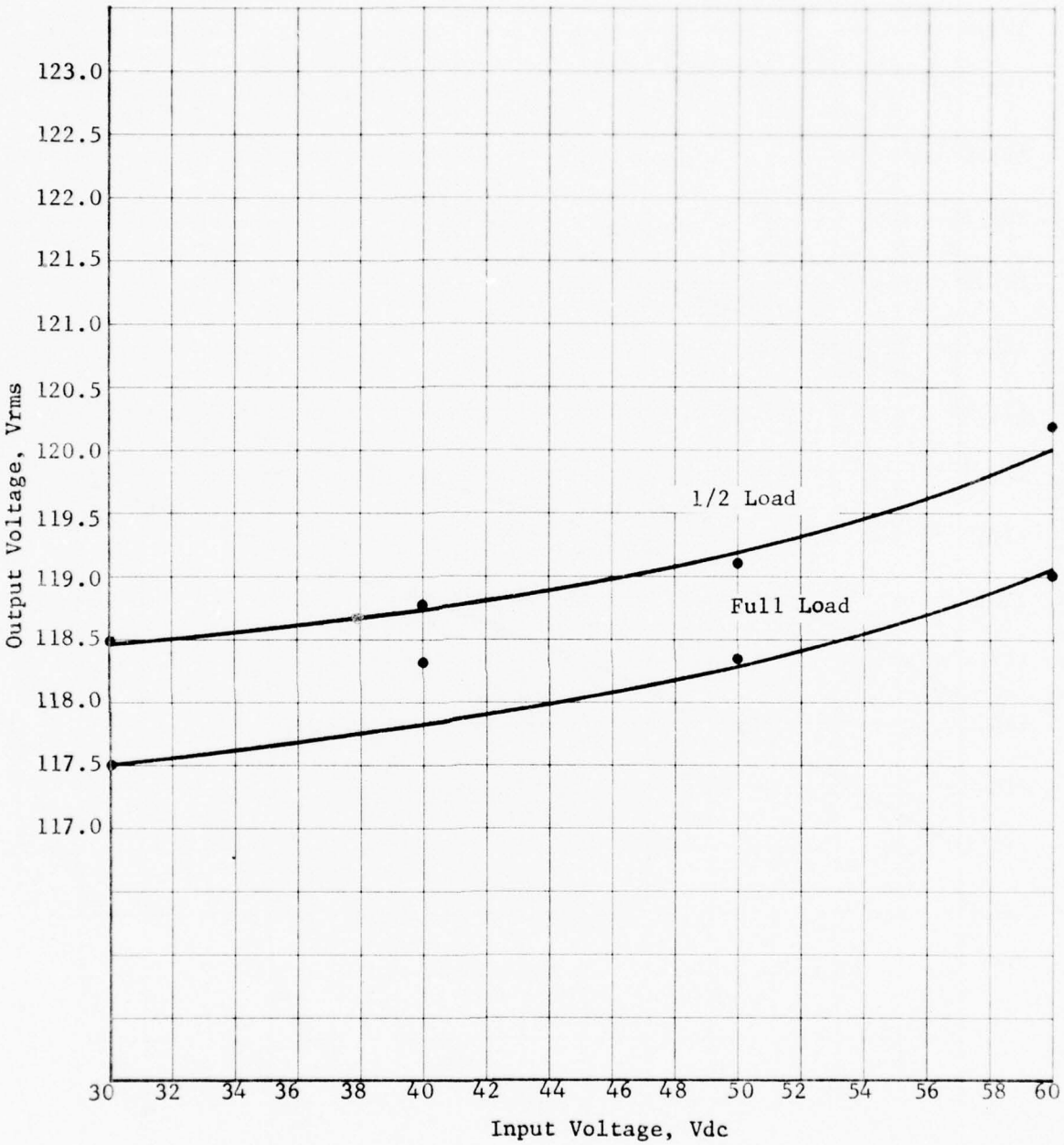


Figure 30. Voltage Regulation - 60 Hz, PF = 0.8.

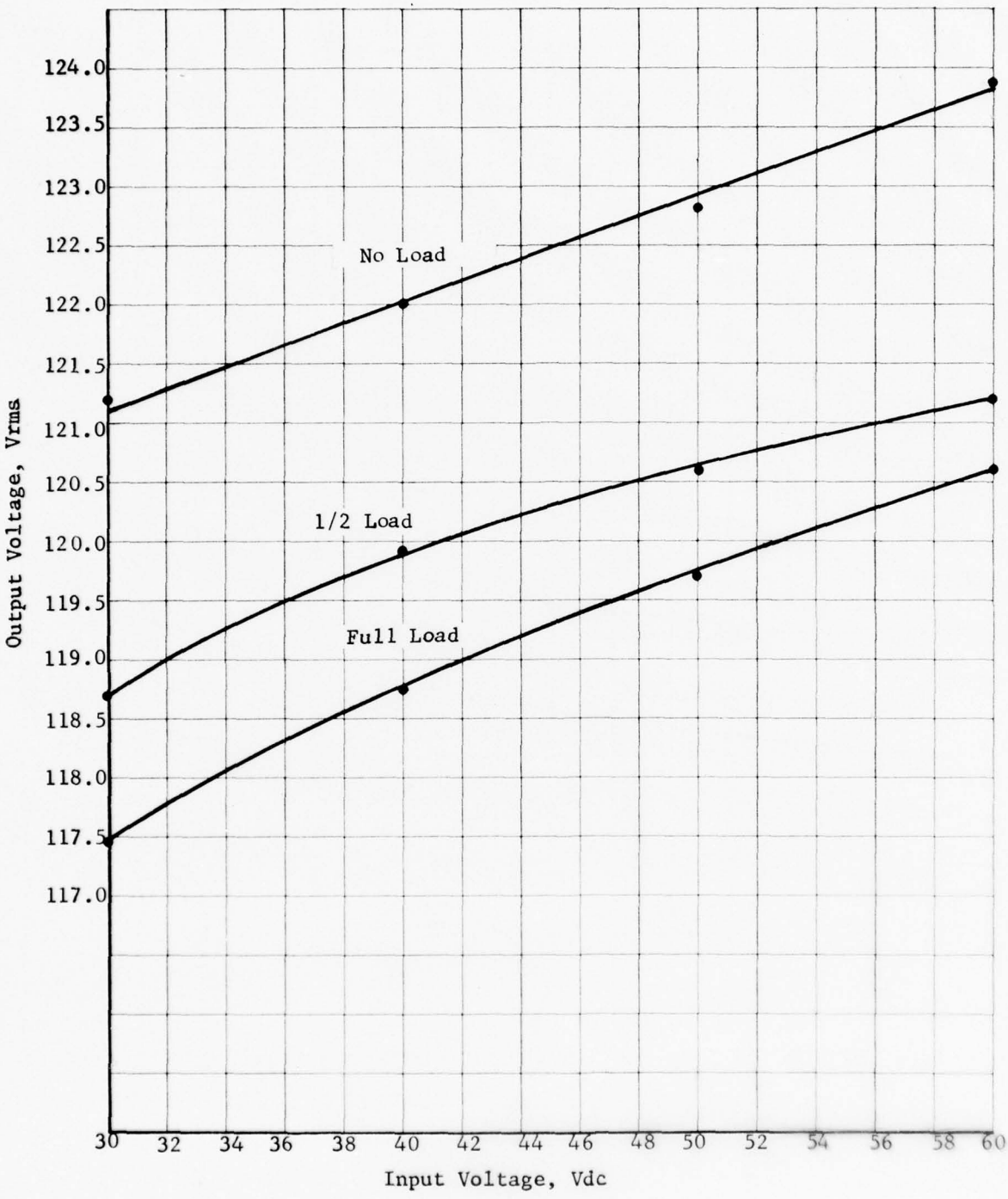


Figure 31. Voltage regulation - 400 Hz, PF = 1.0.

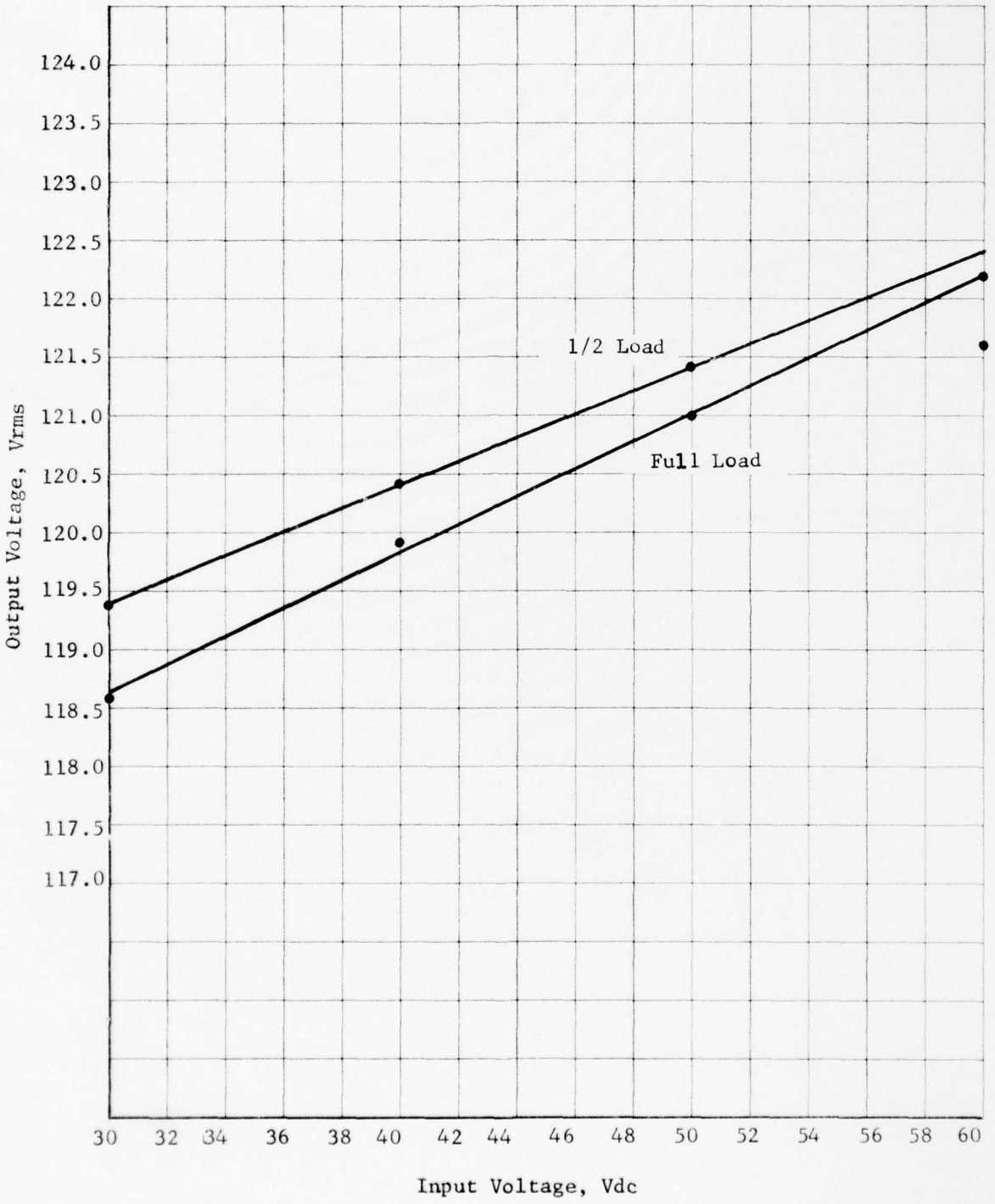


Figure 32. Voltage regulation - 400 Hz, PF = 0.8.

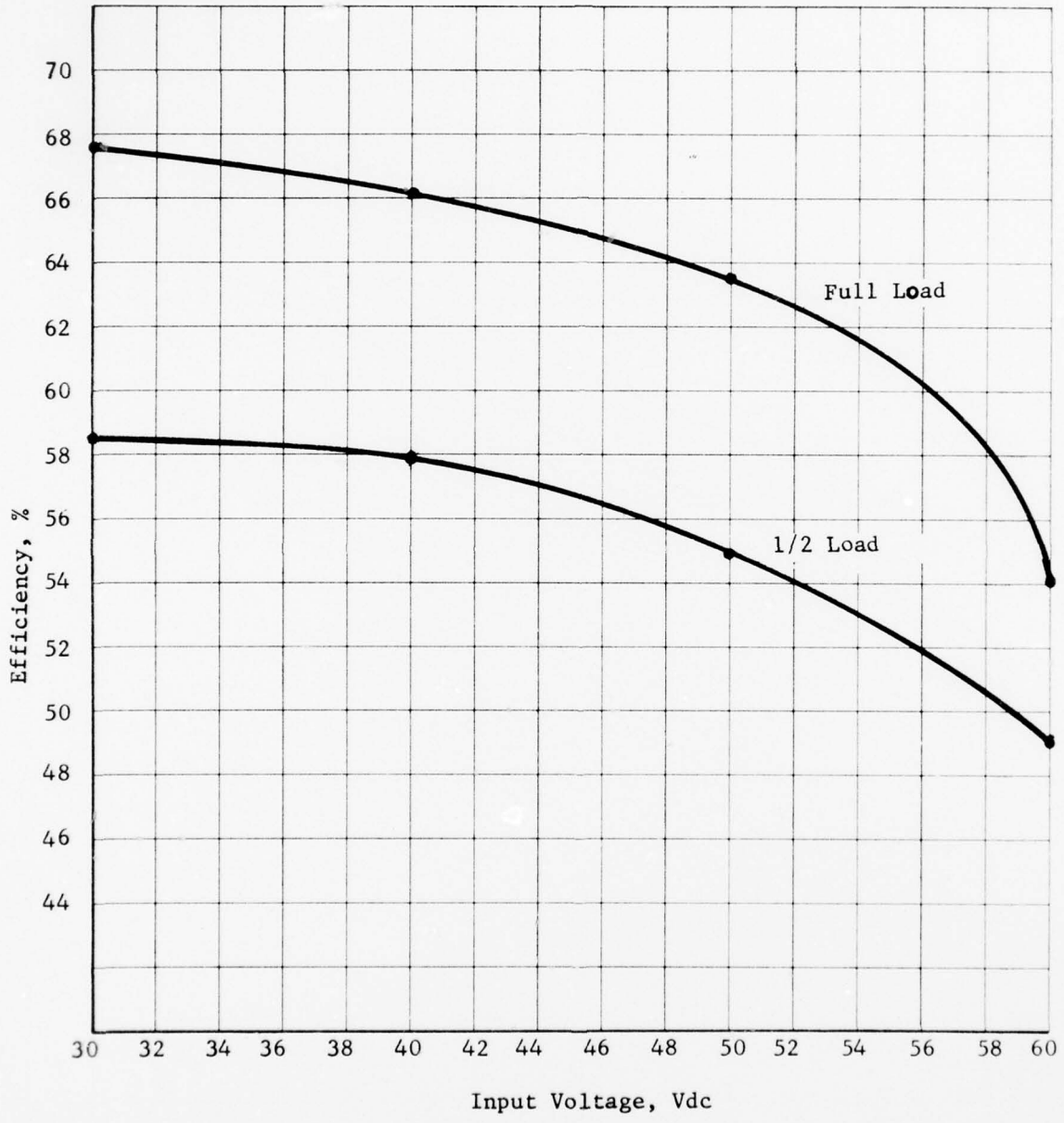


Figure 33. Efficiency - 60 Hz, PF = 1.0.

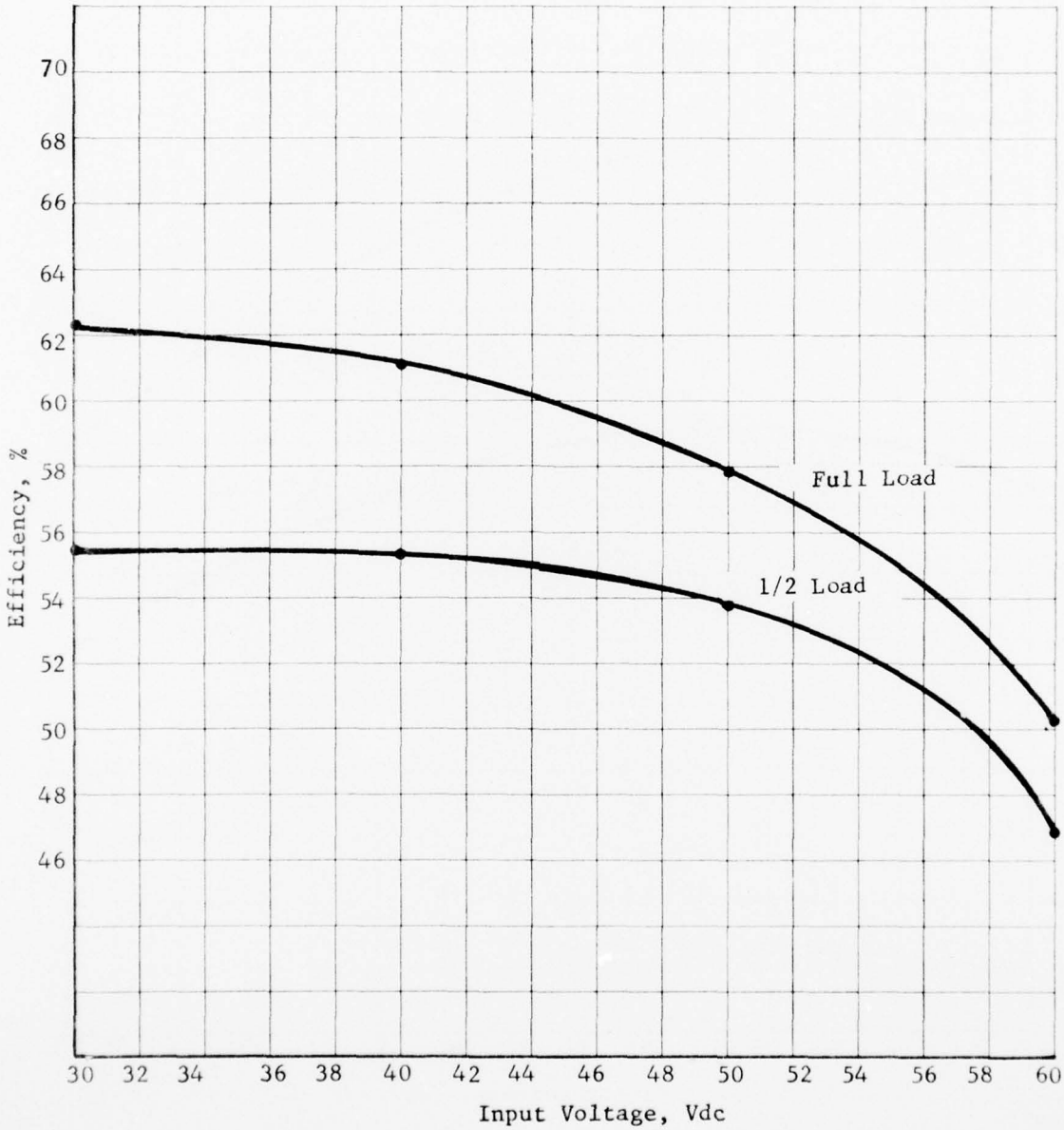


Figure 34. Efficiency - 60 Hz, PF = 0.8.

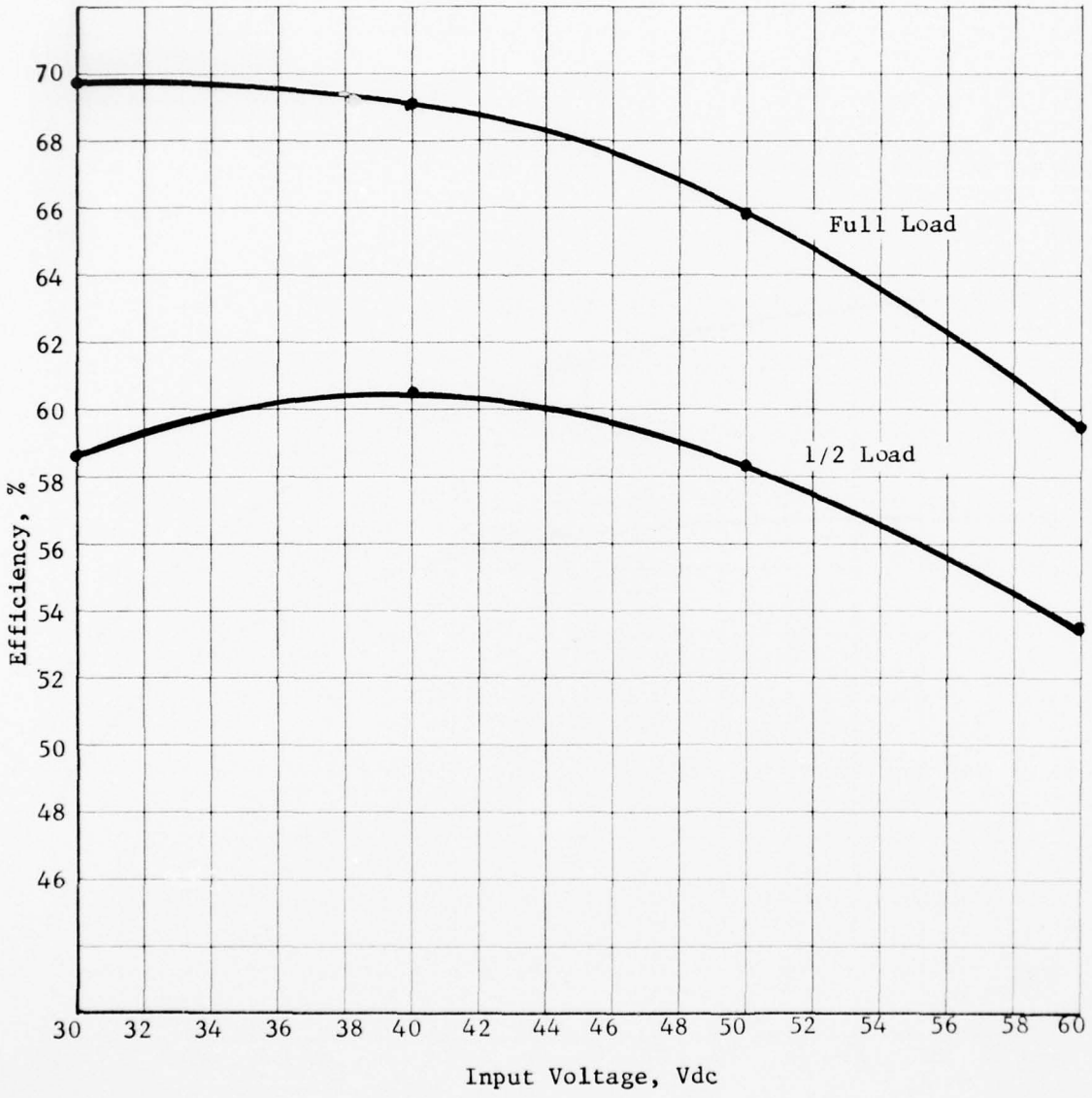


Figure 35. Efficiency - 400 Hz, PF = 1.0.

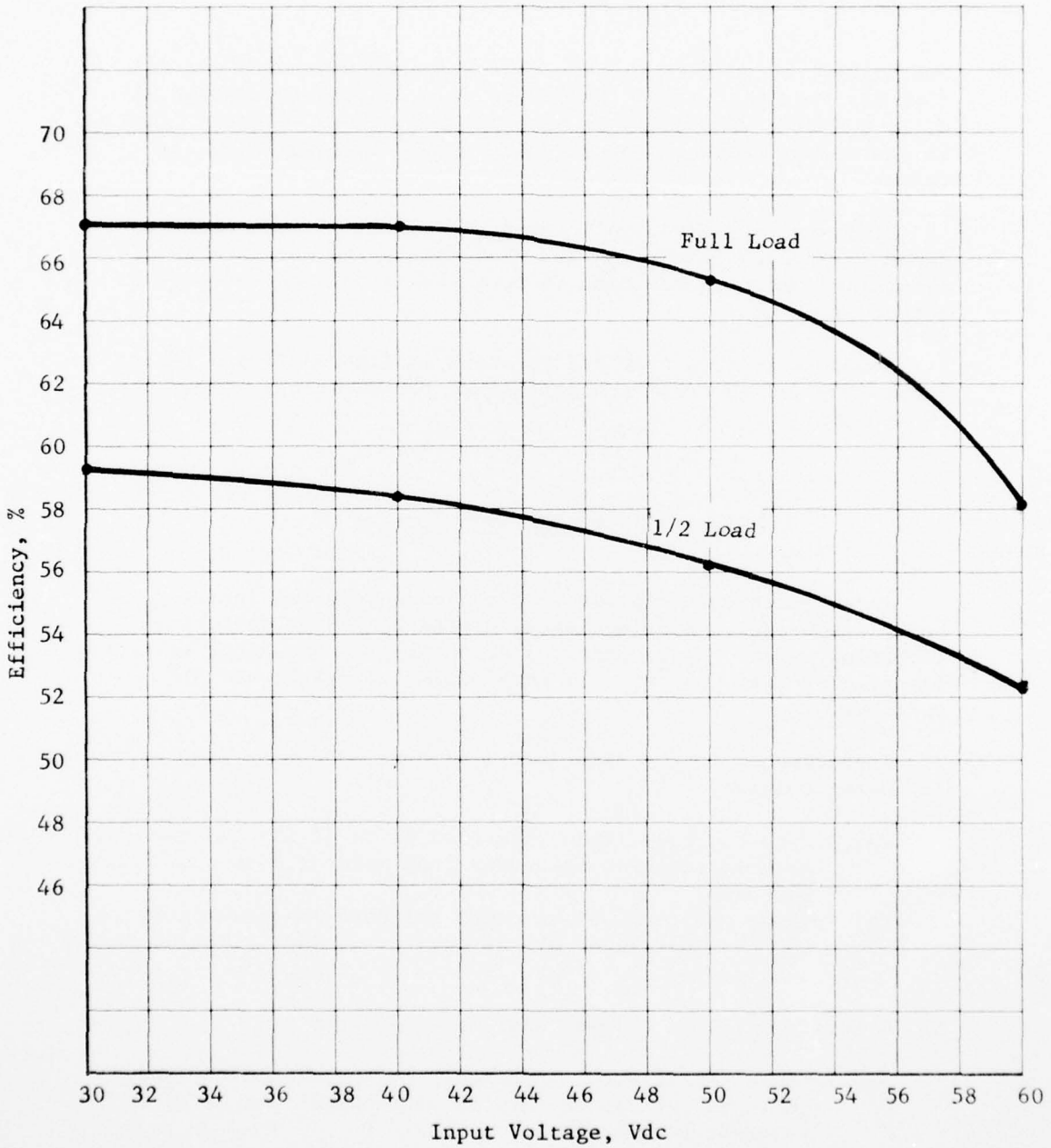


Figure 36. Efficiency - 400 Hz, PF = 0.8.

(a) f_o = 400 Hz, E_{in} = 60 Vdc, PF = 0.8
(b) f_o = 60 Hz, E_{in} = 30 to 60 Vdc, PF = 0.8
(c) f_o = 60 Hz, E_{in} = 60 Vdc, PF = 1.0

The highest third harmonic distortion measurement obtained was 2.4% for case (a) above. Reduction of the harmonic content at 60 Hz and zero load could be accomplished by reducing the damping in the output filter. However, this would increase size and weight.

Response to sudden application on removal of full load, is shown in Figures 19 through 22. Regulation and waveform are maintained and response time is less than a half-period of the output frequency.

Response to 120% overload is shown in Figures 23 and 24. Regulation and waveform are maintained for durations longer than 10 seconds.

Potential Improvements

Three practical versions of the resonant switch inverter power stage can be distinguished, depending on the switching technology used. These versions are: (1) all transitor switches, (2) all SCR switches, and (3) combination transitor and SCR switches.

Improvements in the transistorized version can be made by the following changes.

(a) Reduce the repetition rate from 80 to 40 kHz and the natural resonant frequency from about 150 to about 100 kHz.
(b) Trigger the five 300 VA power switches in sequence at 200 kHz instead of all at once at 40 kHz. This is called interlacing.

The benefits of these changes are expected to be:

(a) Improved efficiency, especially in the magnetics, due to lower repetition rate in each switch and lower resonant frequency.

(b) An effective interlaced repetition rate of 200 kHz instead of only 80 kHz. This will reduce the requirements on the output filter and allow higher damping. This will result in reduced weight in the output filter which at present is one of the main contributors to weight.

Improvements in the silicon-controlled rectifier version can be made as follows:

(a) Increase the repetition rate from 10 to 16 kHz and increase the resonant frequency from 20 to 32 kHz.
(b) Trigger the five 300 VA power switches in sequence at 80 kHz instead of all at once at 16 kHz (interlacing).
(c) Trigger the SCRs on the secondary side of the inverter by using a pulse that lasts only long enough to secure adequate turn-on instead of with a squarewave.

The benefits to be expected from these changes are:

(a) Due to sequential gating of the five power switches, the effective repetition rate will be 80 kHz. This will improve regulation and waveform to the level obtained in the performance test results for the transistorized breadboard unit.
(b) Short pulse triggering of the SCRs on the secondary side of the inverter will improve efficiency of the phase drive function and will also allow the SCRs to be operated at full reverse voltage.

There is a possibility of using transistors in the primary side and SCRs in the secondary side of the inverter with little or no reduction in repetition rate and with sequential triggering for interlacing. The benefit of this approach, compared to the all-transistor version, is simplicity and cost-reduction in the secondary side. This results because six transistors and six diodes would be replaced with two SCRs in each of five power switch modules per phase.

The existing high-speed voltage regulation loop provides good transient response. However, at zero load the regulation deteriorates due to reduced resolution. Regulation could be improved by using an additional regulator loop that senses average output voltage compared to a dc voltage reference.

4. COST ESTIMATE

A cost estimate of the SLEEPS Inverter was performed for a production quantity of 100 units delivered over a 5-month period. The estimate was divided into five major areas: mechanical detail fabrication, general assembly fabrication, test, inspection and material procurement.

An estimate of mechanical detail costs was prepared based on cost-effective production methods. All module assemblies were costed as either sand cast or investment cast aluminum parts. Where appropriate procurement costs were estimated for outside vendor services. The cost estimate included an allowance for planning and supervision and for inspection.

A manufacturing fabrication estimate was prepared based on time standards and improvement curves. Individual fabrication operations were recorded on worksheets. These operations were categorized into run times and setup times. The standard run times were then adjusted by an appropriate improvement curve. A 90 percent improvement curve was used for printed wiring board intensive operations because they allow a degree of automation in the manufacturing process, and an 85 percent improvement curve was used for all other operations. Improvement curves were used to modify run times only. Setup times were not adjusted.

A test estimate was prepared which included test engineering labor, tool fabrication, planning, actual test labor, and material costs.

An inspection estimate was prepared as a fixed percentage of the "hands on" fabrication and test estimates. Different factors were used for the fabrication and test functions. Inspection supervision was then estimated as a fixed percentage of inspection labor.

Material procurement costs were prepared for a 100-unit production quantity. A list of the inverter electronic piece parts is provided in Table 28. The total piece part cost estimate was adjusted by a manufacturing allowance factor to account for scrappage.

The accumulated procurement costs and labor hours established by the methodology described above were modified by standard labor rates for the different labor categories, overhead, general and administrative (G&A), and profit to establish a final cost. For a 100 unit build, the projected cost came to $64,127 per unit recurring and $1984 per unit nonrecurring cost distributed across the 100 units.

TABLE 28. INVERTER PIECE PARTS

Part Number	Manufacturer	Description	Quantity per Machine
Model 4110	Pamotor	Cooling Fan 28 Vdc	3
A-885 Y (Modif.)	Hartman	DC Contactor SPDT 100A, 28V	1
81-1059-01-102	Dialight	Indicator Lamp Assy	6
52-3191	Dialight	Lens, Red	1
52-3192	Dialight	Lens, Green	1
52-3193	Dialight	Lens, Amber	1
52-3194	Dialight	Lens, Blue	1
52-3195	Dialight	Lens, White	1
52-3196	Dialight	Lens, Yellow	1
TT13D-3	Alco Switch	Toggle Switch SPDT	3
28PSB	Chicago Miniature	Lamp 28V, 0.04A (T-2)	6
LM111J/883B	NSC	MicroCircuit, Comparator	13
LM101AJ/883B	NSC	MicroCircuit, Op Amp	9
LM555J/8883B	NSC	MicroCircuit, Timer	4
LM723D/883B	NSC	MicroCircuit, Regulator	1
LM109K/883B	NSC	MicroCircuit, Regulator	1
AF100-2J/883B	NSC	MicroCircuit,Active Filter	3
CD4049MJ/883B	RCA	MicroCircuit, Digital	3
CD4001MJ/883B	RCA	MicroCircuit, Digital	3
CD4013BMJ/883B	RCA	MicroCircuit, Digital	2
CD4023BMJ/883B	RCA	MicroCircuit, Digital	3
CD4027BMJ/883B	RCA	MicroCircuit, Digital	5
CD4040MJ/883B	RCA	MicroCircuit	3
JAN2N2222A	T.I.	Transistor	11
JAN2N2907A	T.I.	Transistor	9
JAN2N3822	Motorola	Transistor, FET	6
JAN2N3792	Motorola	Transistor, Power pNp	2
JAN2N5251	Solitron	Transistor, Power nPn	216
RN65DXXXXF	Dale	Resistor 1/4W, 1% Metal Film	191

TABLE 28. INVERTER PIECE PARTS (continued)

Part Number	Manufacturer	Description	Quantity per Machine
RCR20GXXXM	Allen Bradley	Resistor 1/2W, 5% Carbon	2
RC20G20RM	Allen Bradley	Resistor 20Ω, 1/2W, 5%	6
RWR81S2000FM	Nytronics (Sage)	Resistor 200Ω, 1W (WW) 1%	15
RWR81S10R0FM	Nytronics (Sage)	Resistor 10Ω, 1W (WW) 1%	15
RWR81S5R00FM	Nytronics (Sage)	Resistor 5Ω, 1W (WW) 1%	90
RWR81S1000FM	Nytronics (Sage)	Resistor 100Ω, 1W (WW) 1%	90
JAN1N3813	Motorola	Diode, 12A, 400V	90
JAN1N6076	Semtech	Diode, 6A, 50V	66
JAN1N6079	Semtech	Diode, 12A, 50V	60
JAN1N6081	Semtech	Diode, 12A, 150V	46
Mil-C-39014/02-1230	Aerovox	Capacitor, 0.1 µfd., 100V	12
Mil-C-39014/01-1230	Aerovox	Capacitor, 390 pfd, 200V	2
Mil-C-39014/02-1407	Aerovox	Capacitor 1.0 µfd, 50V	3
Mil-C-39014/01-1555	Aerovox	Capacitor, 0.01 µfd, 100V	4
Mil-C-39022/01-1394	Sprague	Capacitor, 10.0 µfd, 50V	9
M39006/09-8373	Transistor Corporation	Capacitor, 110 µfd, 75V	6
CQR07A1QB-105-J3M	Sprague	Capacitor, 1 µfd, 100V	90
Mil-C-39022/0902	Component Research	Capacitor Filter, Total 330 µfd, 120V	249
CHR01K-287-M	Component Research	Capacitor Filter, Total 130 µfd, 120V	99
M39006/09-8373	Sprague	Capacitor Bank, Tantalum	1110
55036-A2	Magnetics, Inc.	Magnetic Core, Powder	3
55254-A2	Magnetics, Inc.	Magnetic Core, Powder	15
55587-A2	Magnetics, Inc.	Magnetic Core, Powder	15
55115-A2	Magnetics, Inc.	Magnetic Core, Powder	15

TABLE 28. INVERTER PIECE PARTS (concluded)

Part Number	Manufacturer	Description	Quantity per machine
52091-2A	Magnetics, Inc.	Magnetic Core, Tape	3
MC0006-4S	Magnetics, Inc.	Cut C-Core	3
3624-01-00-0	Cambion Series 534	Inductor, Air Core	120
FC11D	Potter Brumfield	Relay Mag. Latch DPDT 6V	1

5. CONCLUSIONS AND RECOMMENDATIONS

Sinewave inverter waveform generation by means of high frequency waveform synthesis is desirable for several reasons. First, potential savings in weight due to the reduced size of key power handling circuit elements operating at high frequency can be projected. In addition, the possibility of single stage power processing is feasible since voltage regulation can theoretically be accomplished by controlling the average number of high frequency pulses delivered to the load circuit. Single stage power processing is itself desirable from the standpoint of reducing overall circuit parts count (hence, reducing weight and cost while increasing reliability) and increasing overall inverter efficiency.

While the desirable features of high frequency synthesis discussed above can potentially be exploited, there are compensating drawbacks inherent in the technique. One drawback pertains to output voltage control at light load. The techniques investigated depended for regulation on controlling the average number of controlled energy pulses to the load circuit. At light load, the number of such pulses in a single output period becomes small and control resolution is degraded. A second drawback is the difficulty of achieving sufficiently high frequency for practical application of the techniques. Present day high power devices, particularly SCRs, have limited frequency capability. Transistors can be used to operate at higher frequency. However, the power handling capability is severely limited. Also, in the SLEEPS application considered, high circuit voltages were generated that required connecting a number of transistors in series to sustain the voltages.

As a consequence of these drawbacks, the circuit techniques investigated do not appear promising for high power inverters.

APPENDIX A

IMPROVEMENT CURVES

The use of improvement curves is an accepted procedure throughout the industry for cost estimating. The technique is also accepted and recommended by government agencies.

The term "learning curve" is perhaps more commonly used than "improvement curve." However, there are subtle nuances of meaning in the terminologies that favor "improvement curve" as more descriptive, because it implies active and aggressive improvement policies and programs rather than passive learning processes. The cost reductions predicted by improvement curves do not happen as a matter of course as production continues. They happen as a result of tooling and procedural improvements, the replacement of inefficient methods with efficient ones, the institution of engineering changes to enhance producibility, tighter production control and procurement policies, and, of course, individual operator learning as he fabricates a succession of units. The improvement curve combines all these factors into a characteristic slope. Every industrial process has a characteristic slope. Some will be characterized by steep slopes and some by relatively flat slopes, but the characteristic slope will continue on indefinitely.

It is sometimes felt that achieving cost reductions which continue indefinitely is unreasonable since the cost will eventually go to zero. This is not the case, however. The quantity of units produced will approach infinity much faster than the cost approaches zero. Consider, for example, a 90 percent improvement curve. Every time the quantity of units is doubled, the cost to produce a unit is reduced 10 percent. If it costs 100 hours to produce the first unit, the cost for units in production would be reduced according to the tabulation.

Unit	Manhours
1	100
2	90
4	81
8	72.9
1,000	35.0
100,000	17.4
1,000,000	12.2

Automated processes are typically characterized by higher improvement curves (90 percent and better) than manual operations since less opportunity for improvement exists. Costs are generally

expressed in labor hours rather than dollars, reflecting the fact that labor is a more fundamental basis of comparison and is free of the complicating factors of varying labor rates and inflation. Often certain classes of labor, such as test time and setup time, are excepted from improvement curve cost reduction predictions and are held constant since little opportunity for improvement is expected. Material costs are, of course, not subject to improvement curve analysis.

Unit Cost

The basic equation of improvement curve analysis is given by

$$T(x) = \frac{TFU}{x^N} \tag{A1}$$

or

$$\text{Log} = [T(x)] = \text{Log}\,[TFU] - N\,\text{Log}\,(x) \tag{A2}$$

where

$T(x)$ = the time or cost for the x-th unit

TFU = Theoretical First Unit Cost

x = the production sequence number of the unit for which the cost is to be found

N = the improvement curve slope factor.

The definition of improvement curve given above is known as the unit straight line system (Crawford) and is the most widely used. One other definition in common usage is the cumulative average straight line system (Wright). The formula for this system is identical to equation A1. However, for the Wright system, $T(x)$ expresses the average time or cost to product a total of x units rather than the cost to produce the x-th unit. The analysis which follows applies only to unit straight line systems.

Improvement curves are, in general, characterized by a performance factor, P, which describes the cost improvement obtained when the quantity of units is doubled. For example, for a 90 percent learning curve (P=0.9), the cost of the second unit will be 90 percent of the cost of the first, the cost of the fourth will be 90 percent of the cost of the second, and so on. The improvement curve slope factor, N, is related to the performance factor, P, by

$$N = - \frac{\text{Log } (P)}{\text{Log } (2)} \qquad \text{(A3)}$$

As an illustration, consider the costs of five production units to a 90 percent improvement curve. The improvement curve slope factor can be found from equation A3 as

$$N = - \frac{\text{Log } (0.9)}{\text{Log } (2)} \qquad \text{(A4)}$$

$$= 0.1520031$$

Individual unit costs can then be found from equation A1, or

$$T(x) = \frac{TFU}{x^{0.1520031}} \qquad \text{(A5)}$$

The individual unit costs are tabulated.

Unit, x	T(x)/TFU
1	1.000
2	0.900
3	0.846
4	0.810
5	0.783

In production estimating, time standards are normally given for a product well into production rather than for the first unit. The theoretical first unit cost, TFU, can be derived from the high production figure to give a starting point in analysis. Consider, for example, a standard run time of 139.65 hours for the 5000th unit and a 90 percent improvement curve. The TFU cost is found by simply rearranging equation A1:

$$TFU = x^N \, T(x)$$

$$= 5000^{0.1520031} \times 139.65$$

$$TFU = 509.67 \text{ hours} \qquad \text{(A6)}$$

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Average Unit Cost

For production cost estimating purposes, the average unit cost for a production run is of more interest than an individual unit cost figure. As an illustration, consider the problem of establishing an average cost for production units 21 through 30 for the case of a 90 percent learning curve. From equation A4, we have

$$N = -\frac{\text{Log } P}{\text{Log } 2}$$

$$= -\frac{\text{Log } 0.9}{\text{Log } 2}$$

$$N = 0.1520031$$

The individual unit costs can be found from equation A1. These costs are tabulated in Table A1. The sum of the costs divided by the 10 units over which they are distributed gives the average unit cost, 0.6119133.

TABLE A1. PRODUCTION COSTS FOR 90% IMPROVEMENT CURVE

Unit, x	T(x)/TFU
21 (a)	0.629533
22	0.625097
23	0.620888
24	0.616884
25	0.613068
26	0.609424
27	0.605938
28	0.602598
29	0.599392
30 (b)	0.596311
Sum =	6.119133
Average =	0.6119133

For large production quantities, the effort involved in calulating individual unit costs, summing the costs for all production units, and averaging the total cost becomes prohibitive. Fortunately, for large quantity analysis, a useful estimating relation can be established. The problem is illustrated in Figure A1. For a production run of units from a to b, the cumulative costs for the production run are represented by the sum of the rectangular areas. The total rectangle area is composed of the area under the curve (shaded portion) and the individual corner areas, A_a through A_b. These corner areas can be approximated as triangular segments with individual areas given by:

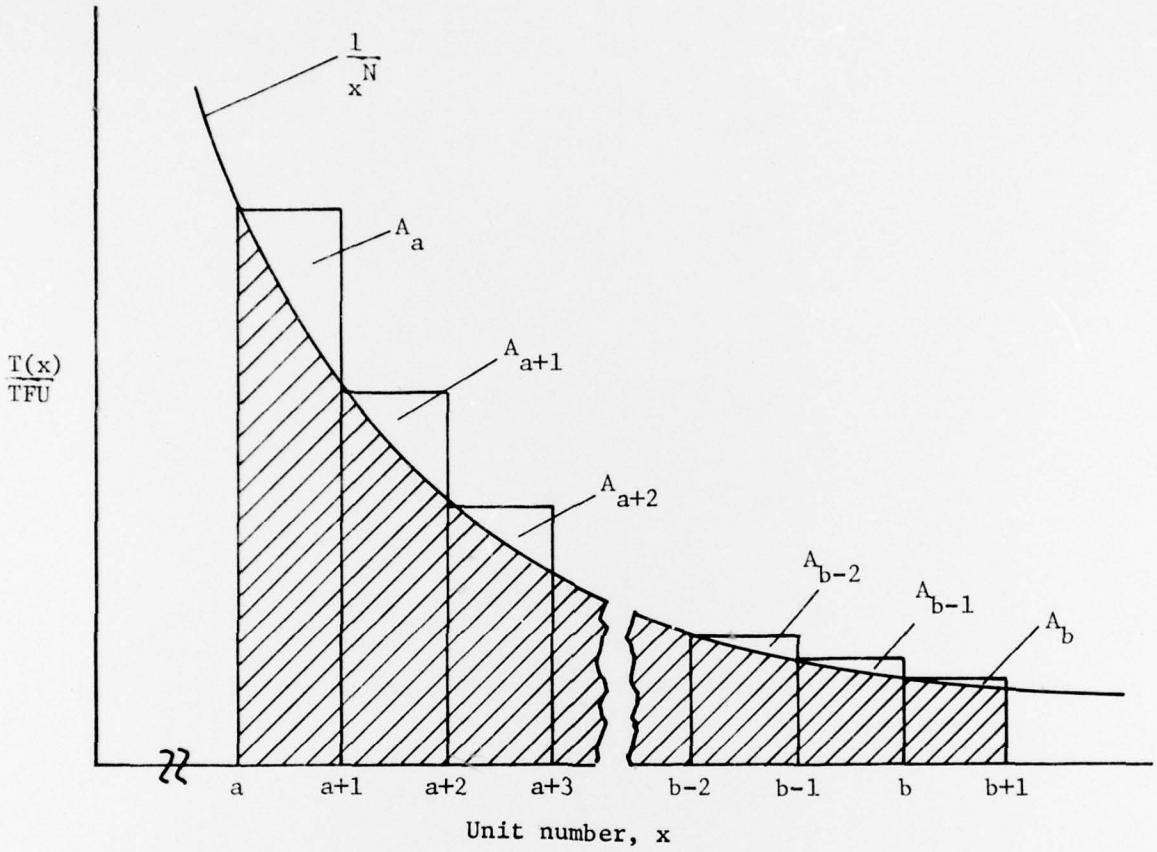

Figure A1. Unit cost curve.

$$A_a = 0.5\left[\frac{1}{a^N} - \frac{1}{(a+1)^N}\right]$$

$$A_{a+1} = 0.5\left[\frac{1}{(a+1)^N} - \frac{1}{(a+2)^N}\right]$$

$$A_{a+2} = 0.5\left[\frac{1}{(a+2)^N} - \frac{1}{(a+3)^N}\right]$$

$$\vdots$$

$$A_{b-2} = 0.5\left[\frac{1}{(b-2)^N} - \frac{1}{(b-1)^N}\right]$$

$$A_{b-1} = 0.5\left[\frac{1}{(b-1)^N} - \frac{1}{b^N}\right]$$

$$A_b = 0.5\left[\frac{1}{b^N} - \frac{1}{(b+1)^N}\right] \qquad \text{(A7)}$$

The sum of all triangular segment area, A_T, can be conveniently expressed by,

$$A_T = A_a + A_{a+1} + \cdots + A_b$$

or

$$A_T = 0.5\left[\frac{1}{a^N} - \frac{1}{(b+1)^N}\right] \qquad \text{(A8)}$$

The shaded area under the curve x^{-N} is found by direct integration.

$$A_c = \int_a^{b+1} \frac{1}{x^N}\, dx$$

$$= \frac{1}{1-n}\, x^{1-N}\Big|_a^{b+1}$$

or

$$A_c = \frac{(b+1)^N - a^{1-N}}{1-N}$$

The estimate of cumulative time represented by the total rectangular area, $T_E(a,b)$, normalized to TFU is then A_T plus A_c, or

$$\frac{T_E(a,b)}{TFU} = \left[\frac{(b+1)^{1-N} - a^{1-N}}{1-N}\right] + 0.5\left[\frac{1}{a^N} - \frac{1}{(b+1)^N}\right] \qquad (A10)$$

Equation A10 provides an accurate estimate of cumulative production costs. For the example given in Table A1, we have for a = 21 and b = 30,

$$\frac{T_E(21,30)}{TFU} = 6.100903 + 0.018093$$

$$= 6.118996$$

which is within 0.002 percent of the actual cumulative cost of 6.119133 given in Table A1.

In general, the error in the approximation given by equation A10 will decrease as the number of units is increased or if the lower limit considered, a, is increased. An upper bound on estimation error can be established by using equation A10 to find the cumulative cost for a single unit, the lower limit unit a. Setting b equal to a in equation A10 gives

$$\frac{T_E(a,a)}{TFU} = \frac{(a+1)^{1-N} - a^{1-N}}{1-N} + 0.5\left[\frac{1}{a^N} - \frac{1}{(a+1)^N}\right] \qquad (A11)$$

Now, the actual cost for this single unit is known to be

$$\frac{T(a)}{TFU} = \frac{1}{a^N}$$

Therefore, we have

$$\frac{T_E(a,a)}{T(a)} = \frac{a^N(a+1)^{1-N} - a}{1-N} + 0.5\left[1-\left(\frac{a}{a+1}\right)^N\right] \qquad (A12)$$

$$= a\left[\frac{a^{(N-1)}(a+1)^{1-N} - 1}{1-N}\right] + 0.5\left[1-\left(\frac{a}{a+1}\right)^N\right]$$

or

$$\frac{T_E(a,b)}{T(a)} = \frac{a\left|\left(\frac{a+1}{a}\right)^{1-N} - 1\right|}{1-N} + 0.5\left|1-\left(\frac{a}{a+1}\right)^N\right| \qquad (A13)$$

For the example of Table A1, equation A13 gives an upper error bound of 0.003 percent. As stated above, the error was actually 0.002 percent. The estimation errors for production runs having several lower limit values of interest are tabulated for a 90 percent improvement curve (N = 0.1520031),

Estimation Error Limit, P = 0.9

a	$T_E(a,a)/T(a) - 1$
1	- 0.66 %
2	- 0.23
5	- 0.048
10	- 0.013
20	- 0.0035
50	- 0.00055
100	- 0.00011

If a production estimate for, let us say, the first 1,000,000 units is desired to better than 0.05 percent accuracy, one can find the individual costs for units 1 through 4 and add them to the cumulative cost estimate given by equation A10 for units 5 through 1,000,000. By equation A13 one is assured that the error is less than 0.048 percent.